

Quartus Prime - Create a new project

- 1. The first step in creating a new project in Quartus Prime is to create a new directory where all project files will be stored. The directory path must not contain spaces or Polish diacritical characters (e.g., a, e, s, etc.).
- 2. You should copy the specified file with the qsf extension into the project directory. This file links the symbolic names of the input/output pins used in the project with the physical pins of the FPGA device.
- 3. Launch the Quartus Prime program and open the New Project Wizard from the welcome window by selecting *Create a New Project (New Project Wizard)* or navigating to *File -> New Project Wizard...* The New Project Wizard window will appear (Fig. 1). Click the **Next** button.

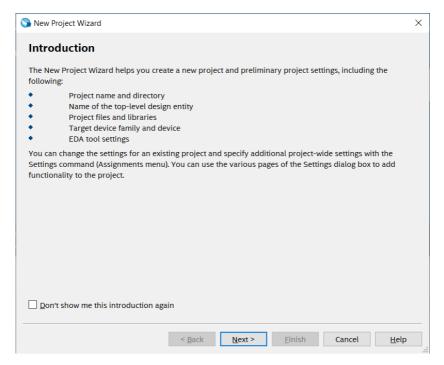


Fig. 1: New Project Wizard - Window 1





4. In the next window (Fig. 2), specify the previously created directory as the project location and enter the project name. The name must not contain spaces and cannot start with a digit. Click the **Next** button.

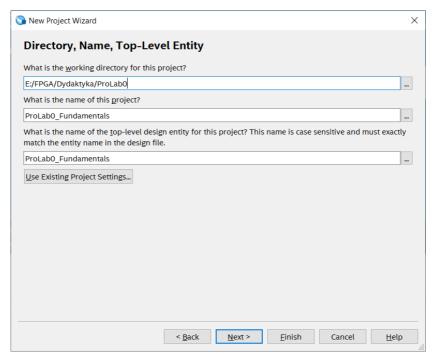


Fig. 2: New Project Wizard - Window 2

5. In the next window (Fig. 3), you should select the "Empty Project" option.

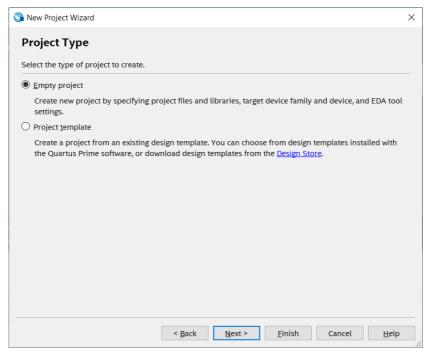


Fig. 3: New Project Wizard - Window 3





6. In the next window (Fig. 4), you can add external (previously created) files to the project. In this case, it is recommended that they be copied to the project directory beforehand. If you are not adding any new files, click the **Next** button.

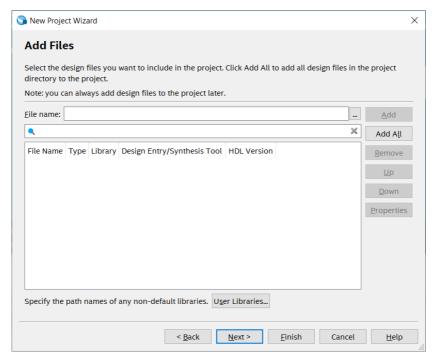


Fig. 4: New Project Wizard - Window 4

7. Next, you need to select the FPGA family and the device that is on the DE10-Lite board. The family and device information can be found on the FPGA itself, the packaging, or the documentation provided by the manufacturer of the DE10-Lite board.

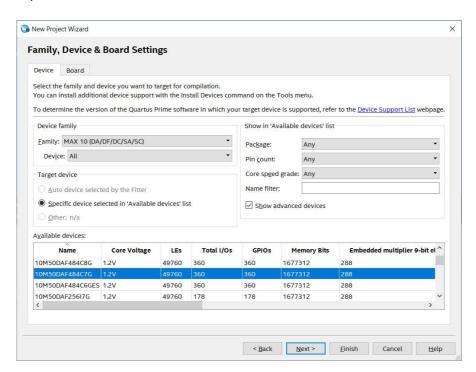


Fig. 5: New Project Wizard – Window 5





8. The next window allows you to configure the integrated helper tools for analysis, synthesis, and simulation. We will leave everything unchanged and click the **Next** button.

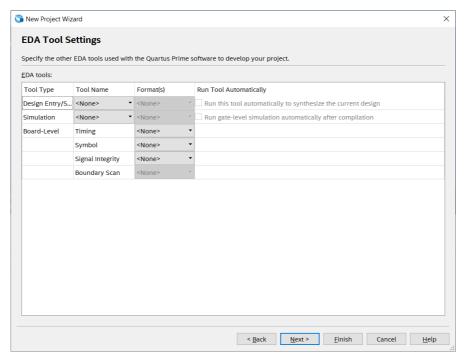


Fig. 6: New Project Wizard – Window 6

9. The last window of the wizard is a summary. If all parameters are correct, click the **Finish** button.

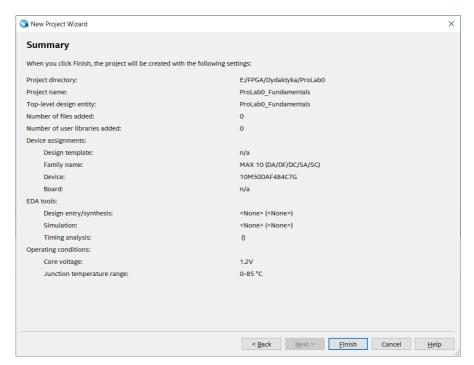
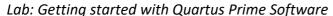


Fig. 7: New Project Wizard - Window 7





10. After completing the project setup wizard, a blank Quartus Prime window should appear (Fig. 8).

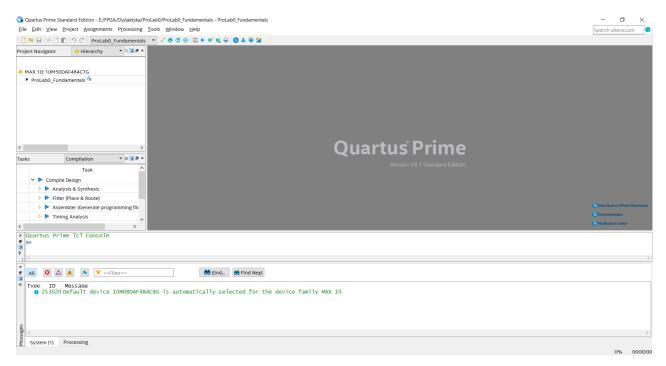


Fig. 8: Quartus Prime Window

11. The next step is to add a block diagram file to the project. To do this, select **File** -> **New**, and then choose **Block Diagram/Schematic File** (Fig. 9).

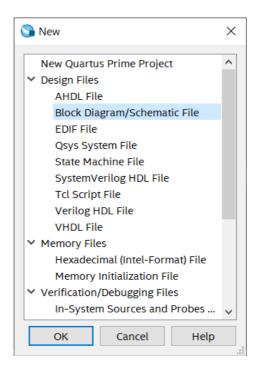
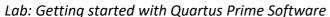


Fig. 9: New file Window





12. A blank block diagram will appear in the main Quartus Prime window (Fig. 10). Next, save the file by selecting File -> Save As... and give it an appropriate name, such as Top.bdf. At this stage, the newly created and saved file should appear in the project's Files tab. The final step is to inform the compiler that this is the top-level file in the project. This is done by selecting the Set as Top-Level Entity option from the menu that appears when you right-click on the file.

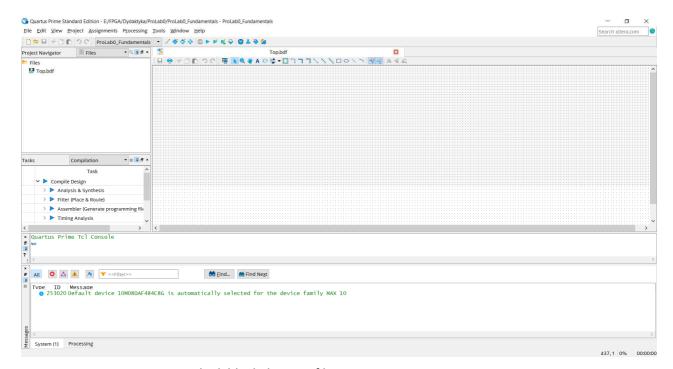


Fig. 10: Blank block diagram file in Quartus Prime

13. The basic elements that can be used to build the diagram are located by clicking on the **Symbol Tool** button (Fig. 11).

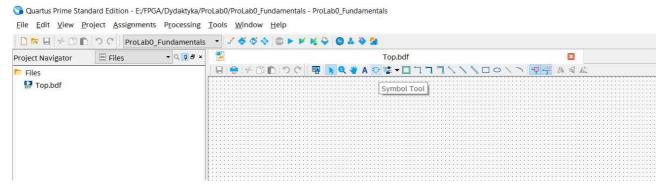
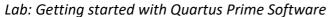


Fig. 11: Symbol Tool





14. To build the simplest project, select one of the available logic gates (Fig. 12).

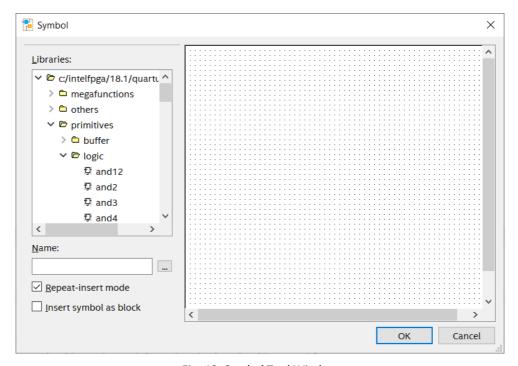


Fig. 12: Symbol Tool Window

15. The next step is to add input/output ports found under the Pin Tool button (Fig. 13).

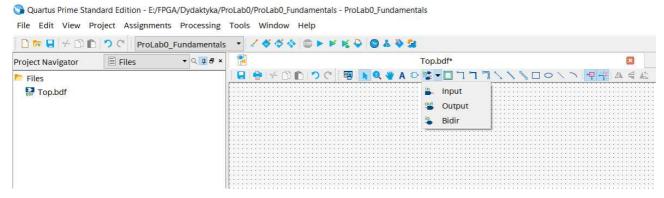


Fig. 13: Pin Tool





16. At this stage, the program window should resemble that shown in Fig. 14. After assigning appropriate symbolic names to the pins (e.g., SW[0], SW[1] as inputs and LEDR[0] as an output), the project is ready for analysis and synthesis. To do this, click the **Start Analysis & Synthesis** button located on the toolbar, or select **Processing** -> **Start** -> **Start Analysis & Synthesis**. At this stage, a correctly built project should have no errors or warnings.

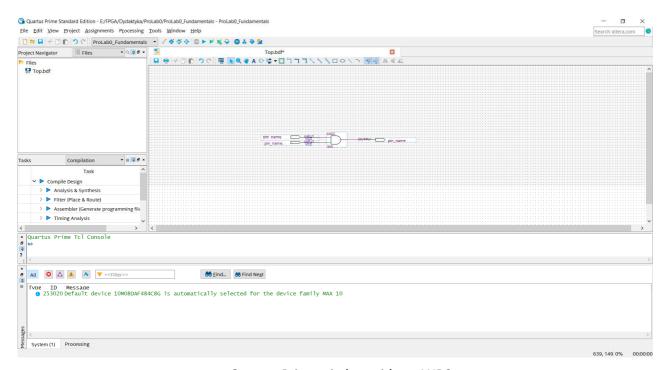


Fig. 14: Quartus Prime window with an AND2 gate

17. Next, you need to import the pin assignments from the qsf file that was previously copied to the project directory. Go to **Assignments** -> **Import Assignments...** This step only needs to be performed once during the project build.

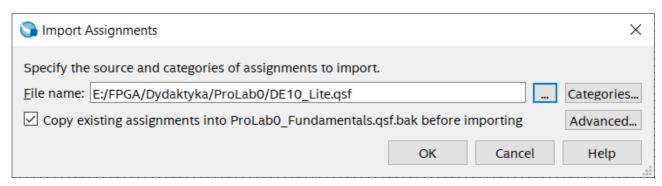
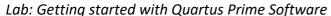


Fig. 15: Import Assignments Window





18. If the previous steps were completed successfully, the block diagram ports should display information about the physical pin numbers of the FPGA device (Fig. 16).

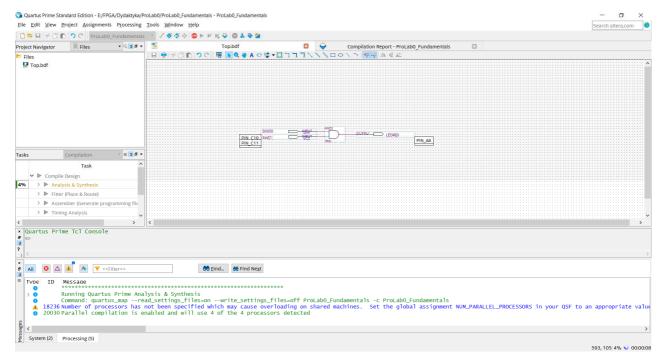


Fig. 16: Quartus Prime Window

19. Before compilation, you still need to set the unused FPGA ports to a high-impedance state. Go to Assignments -> Device -> Device and Pin Options -> Unused Pins -> Reserve all unused pins: As input tri-stated (Fig. 17).

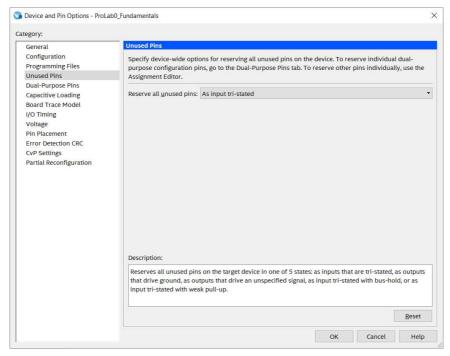
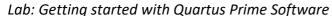


Fig. 17: Device and Pin Options Window





20. To start the project compilation, click the **Start Compilation** button or select **Processing** -> **Start Compilation** (Fig. 18).

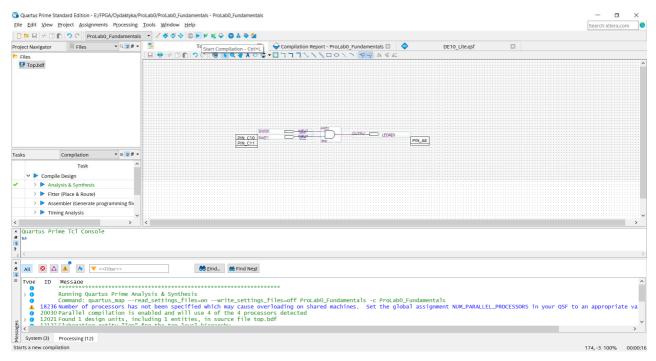


Fig. 18: Quartus Prime window before compilation

21. If the compilation was successful, you can proceed to program the FPGA device. To do this, select the **Programmer** button on the toolbar or go to **Tools** -> **Programmer**. A window will appear as shown in Fig. 19. Next, click the **Add File...** button and select the file with the *.sof extension from the **output_files** subdirectory.

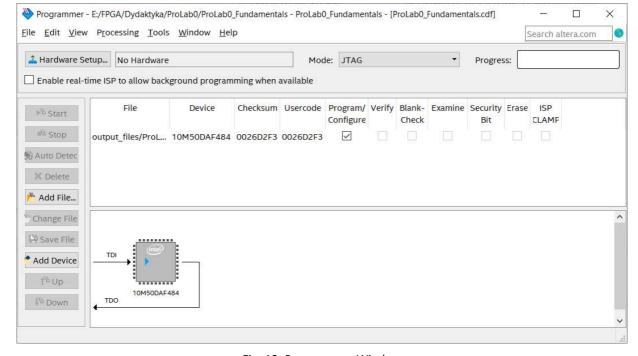
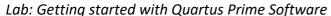


Fig. 19: Programmer Window





22. If the **Start** button is inactive, select **Hardware Setup...** In the window that appears, ensure that **Currently selected hardware: USB-Blaster [USB-0]** is displayed.

If the **Start** button is still inactive, it means that the FPGA device is either powered off, not connected to the computer, or, in the case of using a virtual machine, the physical USB port is not bridged with the operating system in the virtual machine. To program the device, click the **Start** button.

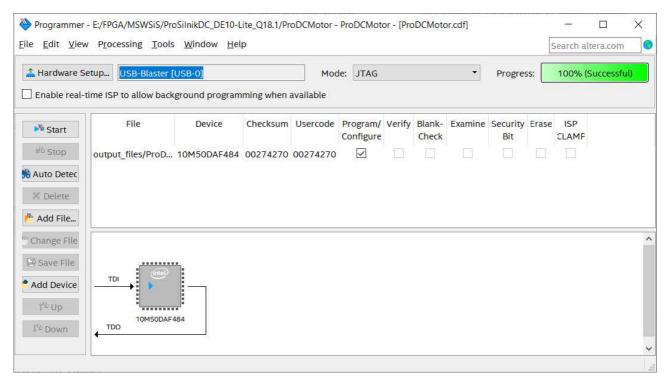


Fig. 20: Programmer tool window after programming the device