THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS

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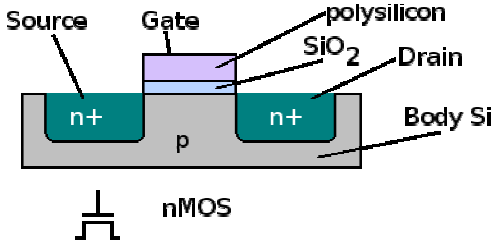
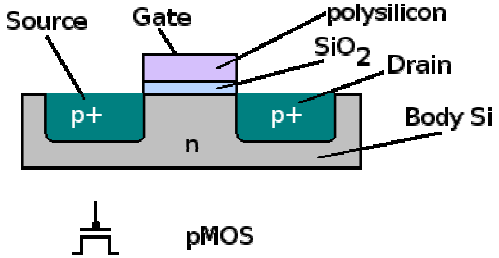
THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS

***DESIGN OF* THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS**

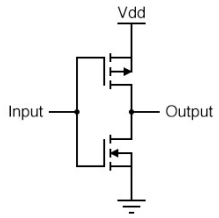
TRANSISTORS
(e.g. N-MOS i P-MOS)



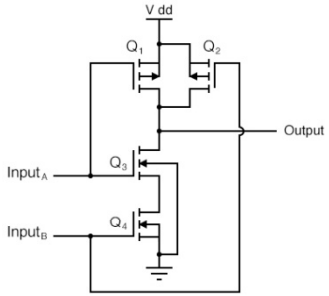


LOGIC GATES AND FLIP-FLOPS
(e.g. NOT, AND, OR)

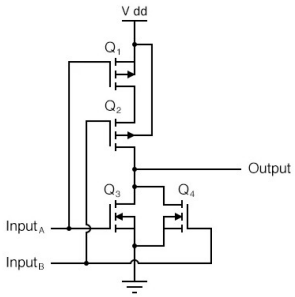
NOT



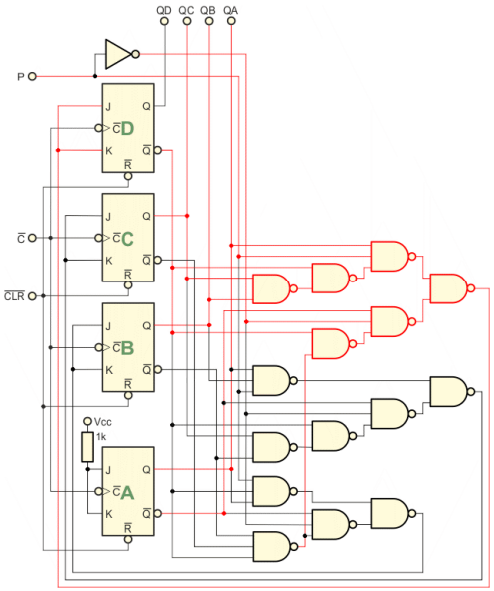
NAND



NOR

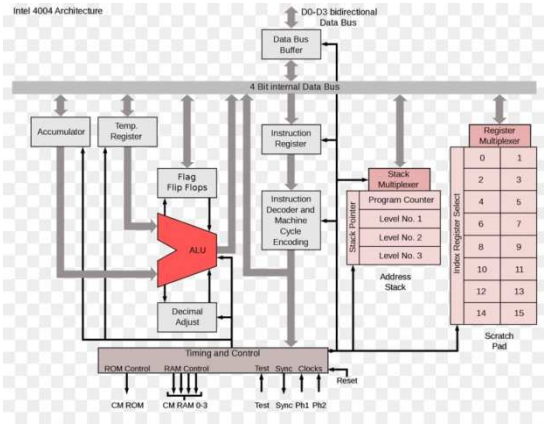


THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS
(e.g. counters, adders, multiplexers, transcoders, state machines)



Mod 5 counter

COMPLEX DIGITAL SYSTEMS
(e.g. ALU, memory controllers, etc.)



THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS

Will knowledge of digital electronics be useful in the future?

FPGA and SoC DEVICES

Knowledge of the design of combinational and sequential logic circuits is **the basic knowledge** regarding the implementation of algorithms in reprogrammable devices as the **FPGA, CPLD**, and hybrid system **SoC (FPGA + processor)**.

ELECTRONICS

- Simple signal operations using 74HC components (eg. replacing one interface with another: A/B to Step/Dir, simple protection systems).

- Low-level programming of microcontrollers (knowledge of the structure of microcontroller peripheral systems).

- Reading and creating diagrams regarding the architecture and operation of digital circuits (counter, multiplexer, comparator, decoder, adder, etc.).

OTHERS

- Knowledge of the building of digital circuits, in particular the processor/microcontroller.

- Knowledge about: 7-segment display construction, PWM modulation, DC motor, control, stepper motor control.

- Developing logical thinking skills. Synthesis of information using a mathematical apparatus.

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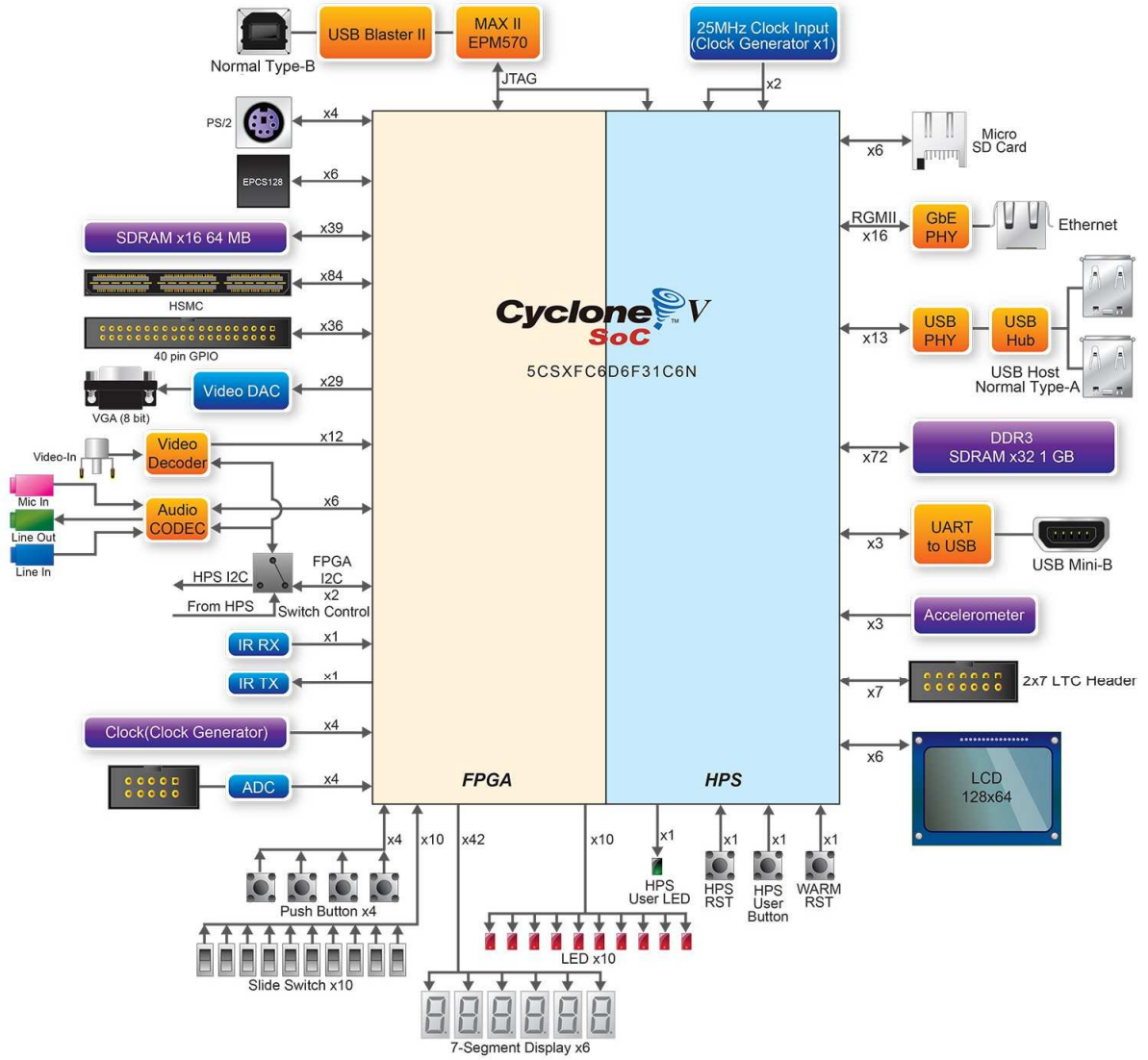

THE COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS

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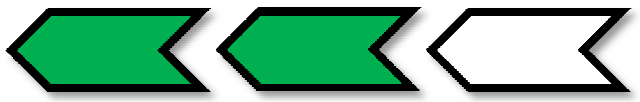

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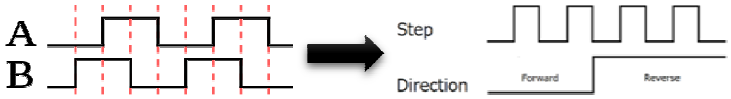

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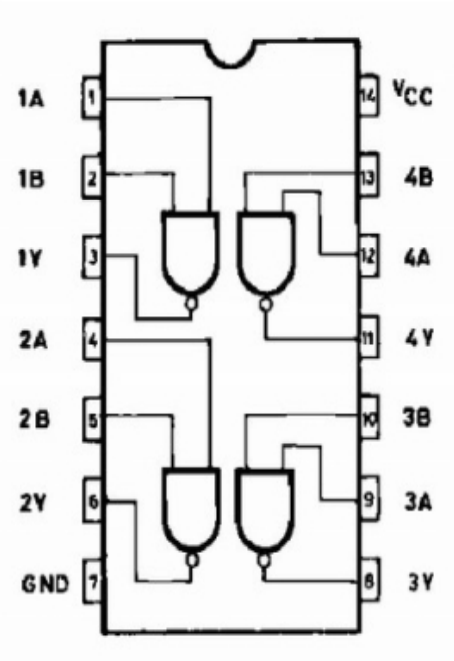
Part No.	Description
74HC00	74HC00 Quad 2-input NAND Gate
74HC02	74HC02 Quad 2-input NOR Gate
74HC04	74HC04 Hex Inverter
74HC08	74HC08 Quad 2-input AND Gate
74HC10	74HC10 Triple 3-input NAND Gate
74HC11	74HC11 Triple 3-input AND Gate
74HC14	74HC14 Hex Inverter Schmitt Trigger
74HC20	74HC20 Dual 4-input NAND Gate
74HC30	74HC30 8-input NAND Gate
74HC32	74HC32 Quad 2-input OR Gate
74HC74	74HC74 Dual D Flip-Flop
74HC75	74HC75 Quad BiStable Transparent Latch
74HC85	74HC85 4-bit Magnitude Comparator
74HC86	74HC86 Quad EXCLUSIVE-OR Gate
74HC107	74HC107 Dual JK Flip-Flop with Reset
74HC123	74HC123 Dual Mono Multivibrator
74HC125	74HC125 Quad Bus Buffer Tri-State
74HC126	74HC126 Quad Buffer/Line Driver, 3-State
74HC132	74HC132 Quad 2-input NAND Schmitt Trigger



The 74HC series is a popular logic family of integrated circuits. The 740HC series contains hundreds of devices that provide everything from basic logic gates, flip-flops, and counters, to special purpose elements e.g: arithmetic logic units (ALU). Specific functions are described in a list of 7400 series integrated circuits.

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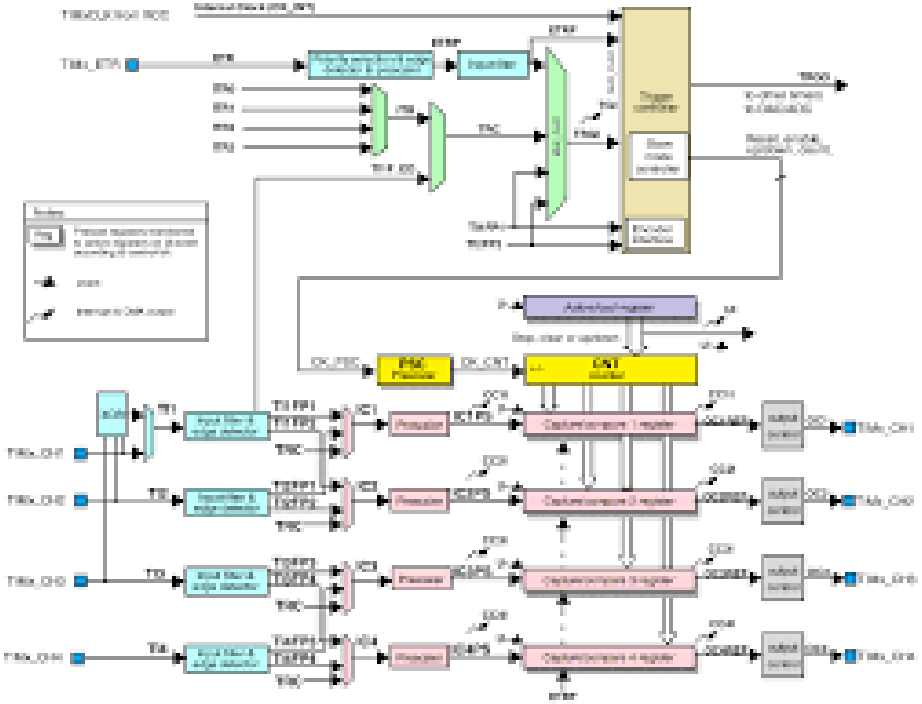
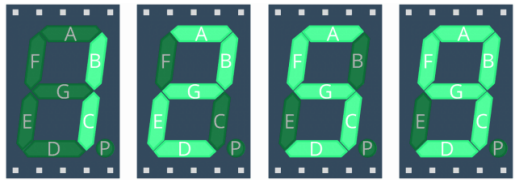
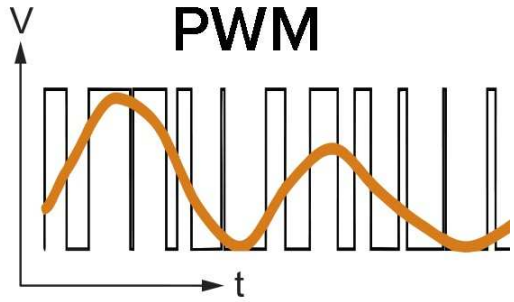
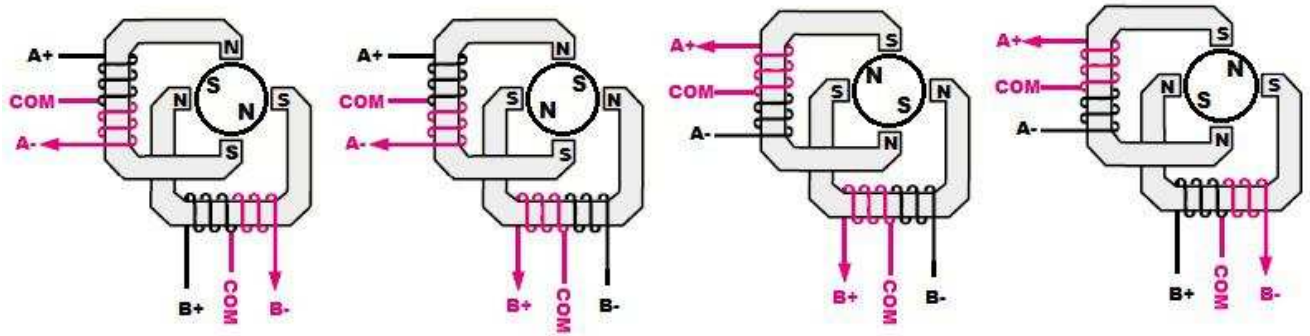








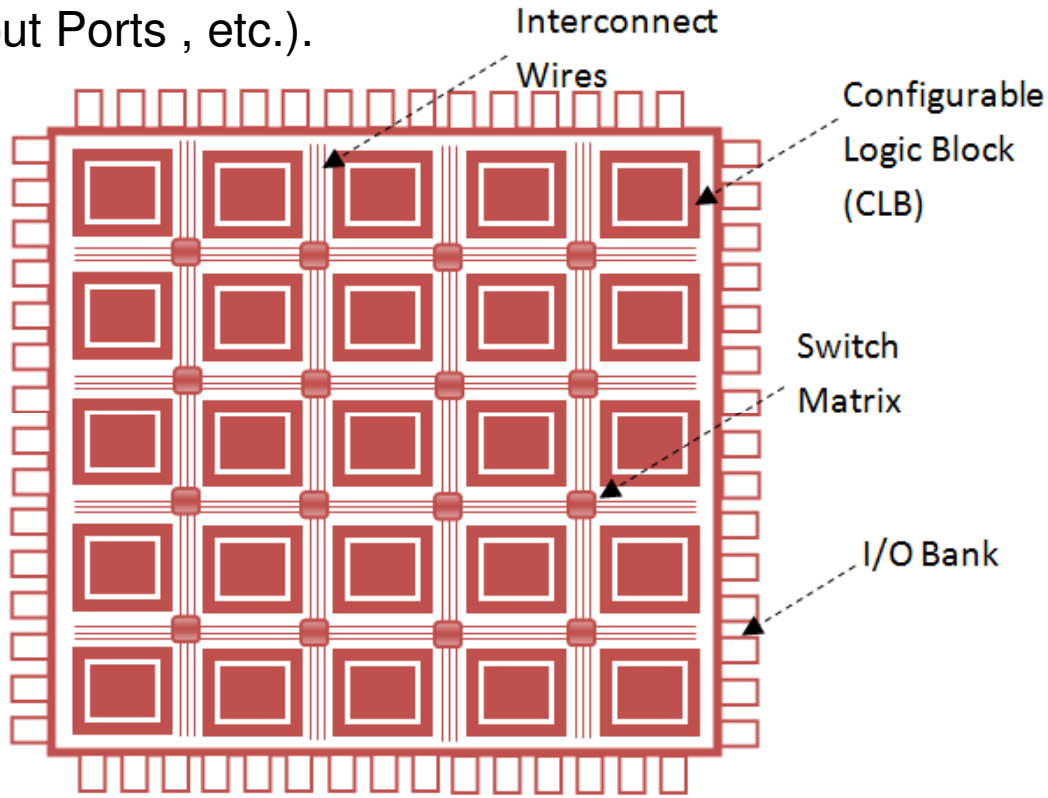
FPGA
(Field Programmable Gate Arrays)

The main components of FPGA devices:

- **LEs cells** *(Logic Elements)* / ***CLBs*** *(Configurable Logic Blocks)*;
- **connection network** – provides local communication with neighboring LEs and global communication within the entire FPGA chip;
- **additional elements** (e.g. memory, multipliers, PLL loops, ADCs , etc.);
- **others** (power system, GPIO - General Input/Output Ports , etc.).

Differences between FPGA devices (and devices' families):

- number of LEs (*Logic Elements*);
- complexity level of LEs;
- device speed (maximum operating frequency, expressed as signal propagation time through LEs ~ 1-9 ns);
- the type and number of integrated equipments (memory, multipliers, PLL loops, ADCs, etc.);
- number of input/output ports - a type of footprint;
- version (commercial/industrial - depending on the operating temperature range).



Companies utilizing FPGA/SoC systems

Companies utilizing FPGA/CPLD/SoC/ VHDL/Verilog technology/skills
operating in Kraków and surrounding areas:

ALDEC
THE DESIGN VERIFICATION COMPANY

WOODWARD

Honeywell

Silicon Creations

intel

Wind Solutions

ARROW ELECTRONICS, INC.

ABB

cadence

ANALOG DEVICES

HITACHI

Hitachi Energy

NOKIA

PREPARATION FOR CLASS

The instructions for each task list the requirements (knowledge and skills) necessary for the correct completion of the exercise.

Actuating, Sensing and Control Mechatronic Systems

Lab: 7-segment display transcoder

7-segment display transcoder

Requirements for the exercise (issues and skills necessary to complete the task):

- representation of numbers in decimal, binary and hexadecimal systems;
- setting up a new project in Quartus Prime;
- creating a hardware module (symbol) in Quartus Prime based on a schematic file (*.bdf);
- creating a hardware module (symbol) in Quartus Prime based on a source code file (eg. *.vhd);
- ability to simplify a logical expressions using the Karnaugh Map method;
- ability to implement a scheme with logic gates based on an algebraic equation.

SCHEDULE

1. ***Combinational logic circuits I***
   Pro: Karnaugh maps exercise.
   Lab: Basic project in Quartus Prime software (implementation of module based on source code file and block diagram / schematic file).

2. ***Combinational logic circuits II***
   Lab: Implementation of combinational logic circuit for seven segment display.
   Pro: implementation of multiplexer;
   implementation of traffic light controller.

3. ***Sequential logic circuits I***
   Lab: Implementation of basic counter;
   design and implementation of individual tasks concerning counters.
   Pro: Implementation of DC motor driver (PWM modulation).

4. ***Sequential logic circuits II***
   Lab: Implementation of basic state machine;
   design and implementation of individual tasks concerning state machines.
   Pro: Stepper motor driver.

PROJECTS

- ***Project tasks:***
  - multiplexer;
  - traffic light controller;
  - DC motor driver (PWM modulator);
  - stepper motor driver.

- ***Project assessment :***
  - operation of the system „on hardware”;
  - **handwritten** notes;
  - answers to questions related to the task (e.g. How does a multiplexer work? What is PWM? How to change the speed/direction of a DC/stepper motor?).

- ***Completion time***

  You can submit your projects for assessment during any class devoted to the implementation of combinational and sequential circuits. You may submit your projects for assessment in every class („on an ongoing basis”) or submit all projects during the final class (dedicated to the implementation of combinational and sequential circuits).

SCHEDULE - POINTS

1. *Combinational logic circuits I (2 p.)*

- homework — *2 p.*

2. *Combinational logic circuits II (8 p.)*

- implementation of 7-segment display controller in FPGA — *4 p.*
- implementation of multiplexer in FPGA — *2 p.*
- implementation of traffic light controller in FPGA — *2 p.*

3. *Sequential logic circuits I (4 p.)*

- implementation of basic counter in FPGA — *1 p.*
- design and implementation of counter with additional input dir (direction of counting up/down), individual task — *1 p.*
- design and implementation of DC motor driver (PWM modulation) — *2 p.*

4. *Sequential logic circuits II (6 p.)*

- implementation of basic state machines in FPGA — *2 p.*
- design and implementation of state machines, individual task — *2 p.*
- design and implementation of stepper motor driver — *2 p.*