7-segment display transcoder

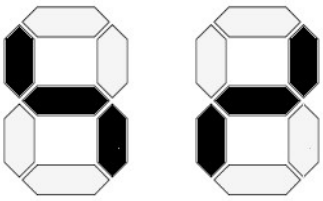
Requirements for the exercise (issues and skills necessary to complete the task):

- **representation of numbers in decimal, binary and hexadecimal systems;**
- **setting up a new project in Quartus Prime;**
- **creating a hardware module (symbol) in Quartus Prime based on a schematic file (*.bdf);**
- **creating a hardware module (symbol) in Quartus Prime based on a source code file (eg. *.vhd);**
- **ability to simplify a logical expressions using the Karnaugh Map method;**
- **ability to implement a scheme with logic gates based on an algebraic equation.**

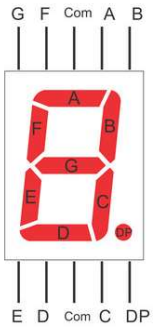
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001

Example:

Design combinational logic circuit to control a 7-segment display. The input is a 4-bit number in BCD format. On the outputs have to appear seven signals to control each display's diodes. Furthermore, for the bit combination 1010 and 1011 on display have to appear special character. The other combinations of bits (1100, 1101, 1110, 1111) don't belong to the domain of the function. **Design the system in the form of a schematic with logic gates.**



1010 1011



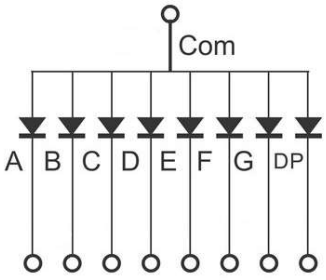


Fig. 1: 7-segment display with a common anode

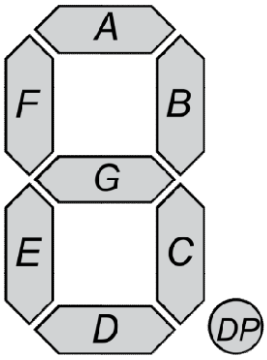


Fig. 2: Arrangement of the segments

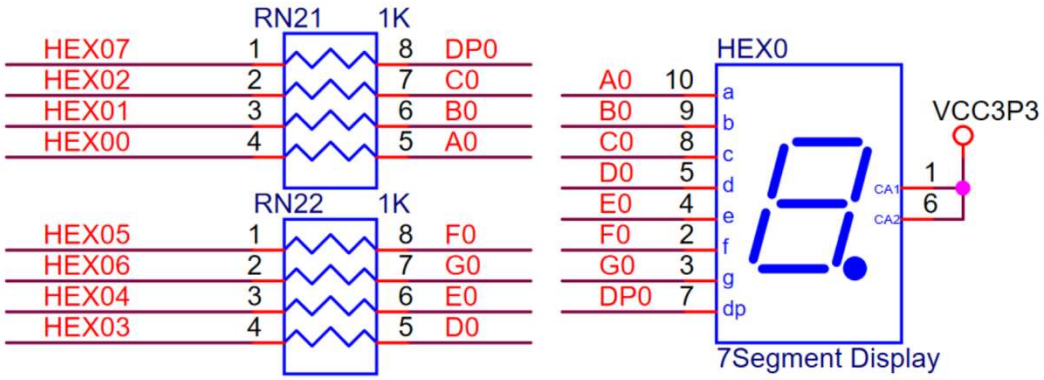
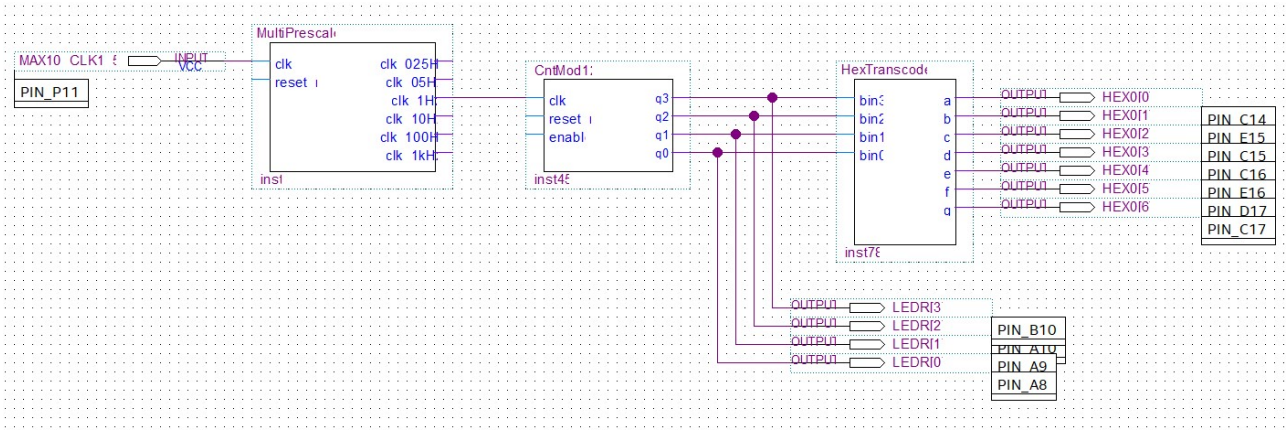
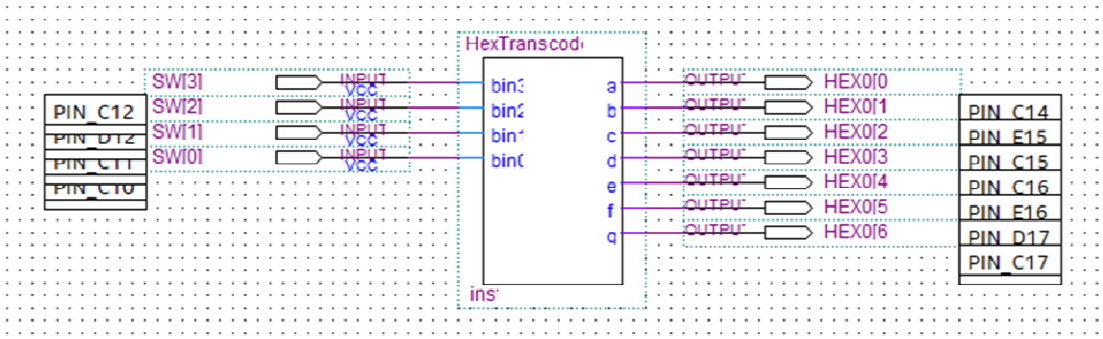


Fig. 3: The electrical connection of the 7-segment display on the DE10-Lite board

In order to test the 7-segment display transcoder use ***MultiPrescaler*** and ***CntMod12*** (counter mod 12). Connect modules as in the picture below.



Another possibility to test the implemented module is to connect the switches (SW[3..0]) directly to the inputs, as shown in the picture below.



Transcoder circuit implement as hardware block (create symbol) ***(4 pts)***:

a) correct project assumption and display connection: ***0.5 pts***;
b) displayed correctly at least 6 characters on display: ***2 pts***;
c) displayed correctly all characters: ***3.5 pts***;
d) created the hardware block (symbol file): ***+0.5 pts***.