SYNCHRONOUS COUNTER DESIGN

A synchronous counter is kind of counter (in contrast to an asynchronous counter) whose output bits change state simultaneously, with no ripple. The only way we can build such a counter circuit is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time. Procedure to design synchronous counter are as follows.

Designing synchronous mod 5 counter using D Flip Flops, counting up.

1. Create state transition table for counter:

***S_n* (Present state)**				***S_{n+1}* (Next state)**			
Q_{DEC}	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_{DEC}
0	0	0	0	0	0	1	1
1	0	0	1	0	1	0	2
2	0	1	0	0	1	1	3
3	0	1	1	1	0	0	4
4	1	0	0	0	0	0	0

2. Determine number of Flip-Flops used.

3. Using state transition table for counter and Flip-Flop excitation table create and simplify the function of each Flip-Flop input using Karnaugh map.

D Flip-Flop excitation table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Karnaugh map for D_0:

$Q_2 \setminus Q_1 Q_0$	0 0	0 1	1 1	1 0
0	1	0	0	1
1	0	-	-	-

$$D_0 = \overline{Q_0}\,\overline{Q_2} = \overline{Q_0 + Q_2}$$

Karnaugh map for D1:

$Q_2 \setminus Q_1 Q_0$	0 0	0 1	1 1	1 0
0	0	1	0	1
1	0	-	-	-

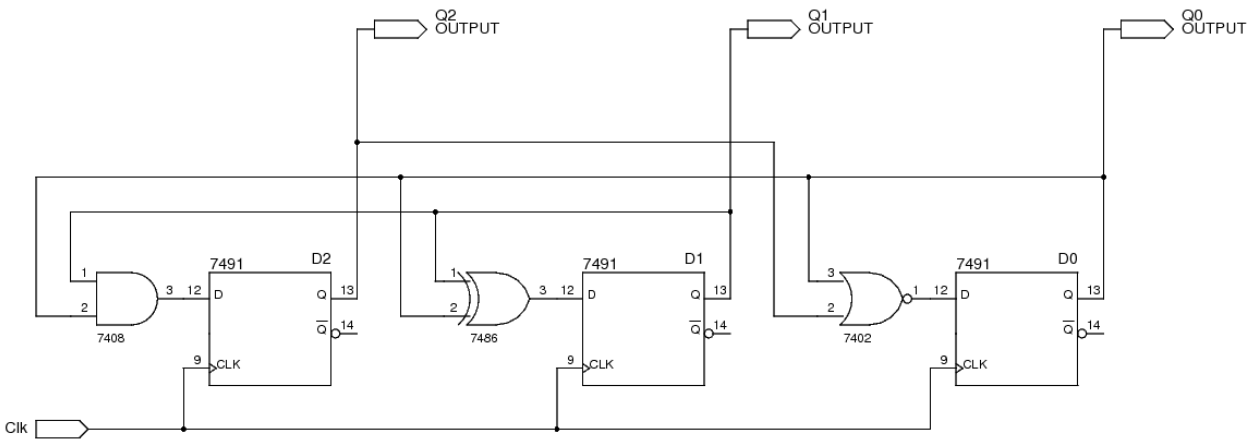
$$D_1 = Q_0\overline{Q_1} + \overline{Q_0}Q_1$$

Karnaugh map for D2:

$Q_2 \setminus Q_1 Q_0$	0 0	0 1	1 1	1 0
0	0	0	1	0
1	0	-	-	-

$$D_2 = Q_0 Q_1$$

4. Draw the circuit.



Rys 1: *Mod 5 counter*

T Flip-Flop excitation table:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

JK *Flip-Flop excitation table:*

Q_n	Q_{n+1}	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0