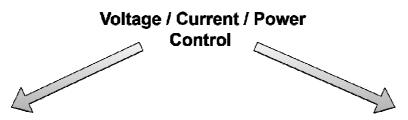
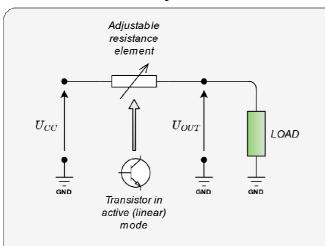


### **PWM Modulation**

PWM modulation is a commonly used method of generating control signals in impulse systems. The PWM signal has a fixed frequency and amplitude, the variable parameter is the pulse width (duty).



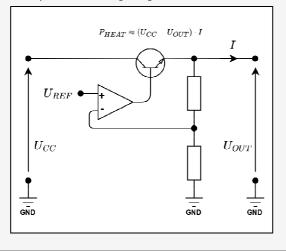
# **Linear Systems**



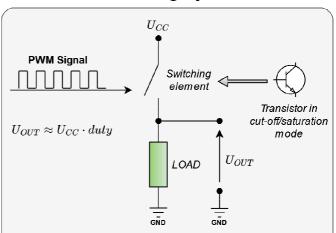
### Applications:

- linear voltage regulators;
- linear power supplies;
- acoustic amplifiers (in A/AB/B class);
- power stages of piezoelectric transducers.

### Example: Linear Voltage Regulator



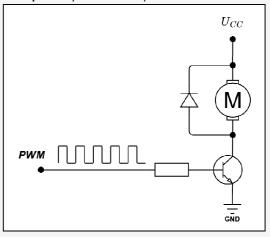
# **Switching Systems**



### Applications:

- switching voltage regulators;
- DC-DC converters;
- switching power supplies;
- acoustic amplifiers (in D class);
- AC/PMSM/BLDC Motors inverters
- DC/Stepper Motors drivers and power stages.

#### Example: Simple DC Motor Speed Controller



## **Actuating, Sensing and Control Mechatronic Systems**

Lab: Sequential Logic Circuits II - PWM



### **Advantages:**

- simpler and more robust construction;
- low level of generated ripples and interference EMC/EMI;
- cheap for low power applications.

### **Disadvantages:**

- low efficiency (~50%);
- low power-to-weight (and power-to-volume) ratio for high power applications;
- expensive solution for high power applications.

### **Advantages:**

- high efficiency (~80 90%);
- good power-to-weight (and power-to-volume) ratio:
- cheap solution for high power applications.

### Disadvantages:

- more complex construction;
- high level of generated ripples and interference EMC/EMI.

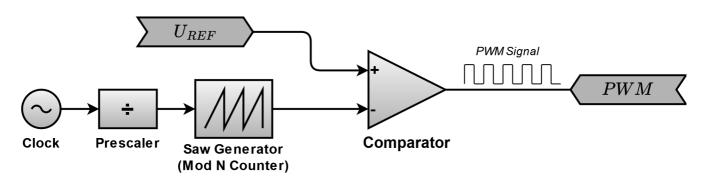


Fig. 1: Block diagram of a PWM modulator

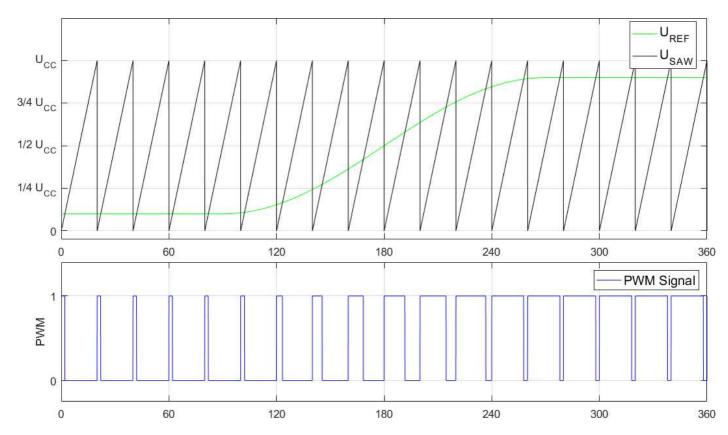


Fig. 2: The principle of generating the PWM signal



### **TASK**

Design and implement n the FPGA device a PWM modulator consisting of a MultiPrescaler module, a mod 16 counter and a 4-bit comparator. Build the mod 16 counter using flip-flops configured in the toggle mode, as in Fig. 3. Implement the 4-bit comparator based on the Karnaugh map placed below (Table 1). As a reference value for the modulator, use a 4-bit number read from the SW[3..0] switches located on the DE10-Lite board.

In order to test the PWM modulator, connect the output signal to the 7-segment display diodes (e.g. HEXO[6..0]) via an additional NOT gate. The duty (pulse width) of the PWM signal will cause a change he brightness of the display segments. Additionally, connect the PWM signal to the GPIO0 and GPIO1 outputs in order to present the signal on the oscilloscope screen or use it to control an external object. Figure 4 shows the final diagram of the PWM modulator in Quartus Prime.

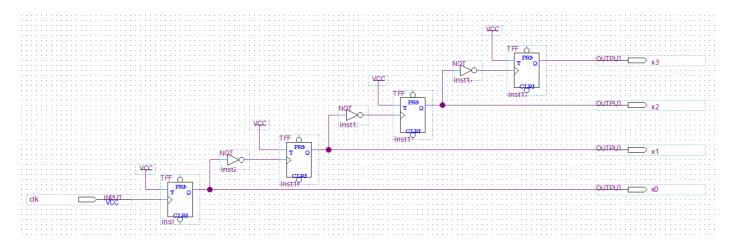


Fig. 3: Counter counting up mod 16

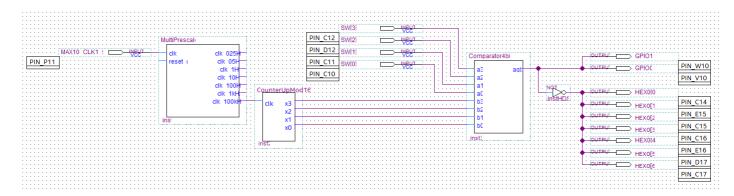


Fig. 4: Schematic of the PWM modulator in Quartus Prime

# **Actuating, Sensing and Control Mechatronic Systems**

Lab: Sequential Logic Circuits II – PWM



Is A > B ? (1 - Yes, 0 - No)  $A_{DEC} = (a_3 a_2 a_1 a_0)_{BIN};$  $B_{DEC} = (b_3 b_2 b_1 b_0)_{BIN};$ 

$b_3 b_2 b_1 b_0$ $a_3 a_2 a_1 a_0$	0000 (0 <sub>DEC</sub> )	0001 (1 <sub>DEC</sub> )	0011 (3 <sub>DEC</sub> )	0010 (2 <sub>DEC</sub> )	0110 (6 <sub>DEC</sub> )	0111 (7 <sub>DEC</sub> )	0101 (5 <sub>dec</sub> )	0100 (4 <sub>DEC</sub> )		1101 (13 <sub>dec</sub> )		1110 (14 <sub>DEC</sub> )	1010 (10 <sub>dec</sub> )		1001 (9 <sub>DEC</sub> )	1000 (8 <sub>DEC</sub> )
0000 (0 <sub>DEC</sub> )	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0001 (1 <sub>DEC</sub> )	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0011 (3 <sub>DEC</sub> )	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0010 (2 <sub>DEC</sub> )	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0110 (6 <sub>DEC</sub> )	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
0111 (7 <sub>DEC</sub> )	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
0101 (5 <sub>DEC</sub> )	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
0100 (4 <sub>DEC</sub> )	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1100 (12 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
1101 (13 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
1111 (15 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1110 (14 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
1010 (10 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1
1011 (11 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
1001 (9 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
1000 (8 <sub>DEC</sub> )	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Tab. 1: Karnaugh map of the 4-bit comparator