Combinational circuits in VHDL

Below is an example of a schematic of a full adder combination circuit and its equivalent in VHDL language.

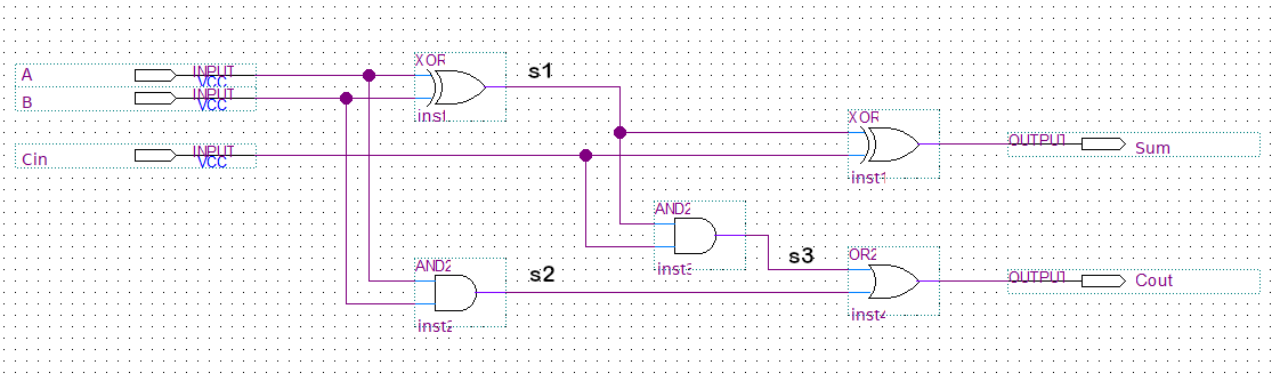

Fig. 1: Logic diagram of a full adder

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4
5   entity FullAdderVhdl is
6      port(
7            A, B, Cin : in std_logic;
8            Sum, Cout : out std_logic
9      );
10  end entity;
11
12
13  architecture FullAdderVhdl of FullAdderVhdl is
14
15     -- Signals declaration
16     signal s1, s2, s3 : std_logic := '0';
17
18  begin
19
20     s1 <= A xor B;
21     s2 <= A and B;
22     s3 <= s1 and Cin;
23     Sum <= Cin xor s1;
24     Cout <= s2 or s3;
25
26     -- Example of AND4
27     -- s100 <= s101 and s102 and s103 and s104;
28
29     -- Example of OR4
30     -- s100 <= s101 or s102 or s103 or s104;
31
32  end architecture;
33
```