Actuating, Sensing and Control Mechatronic Systems

Memories

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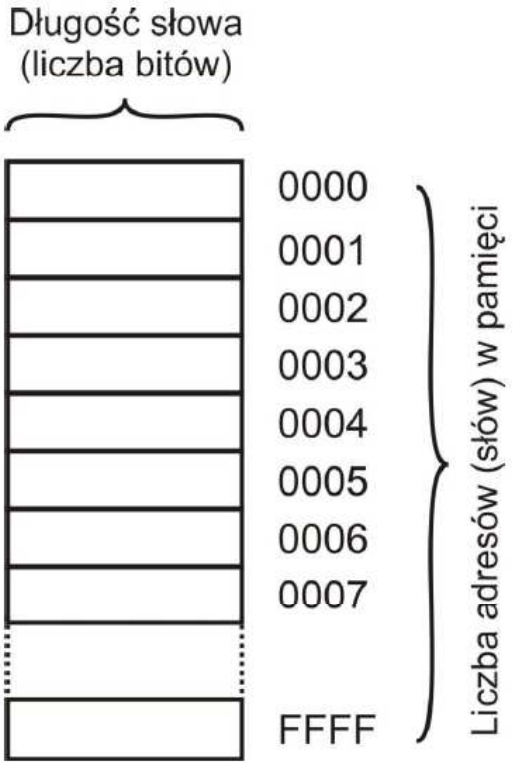
AGENDA

1. Memories (definitions, basic information)
2. Classification of memory
3. Nonvolatile - ROM (Read Only Memory)
   a) MROM
   b) PROM
   c) EPROM
   d) EEPROM
   e) FLASH
4. Volatile - RAM (Random Access Memory)
   a) SRAM
   b) SSRAM
   c) DRAM
   d) SDRAM
   e) DDRx (Double Data Rate)
5. Summary

Memories
Basic definitions



Semiconductor memory is a digital electronic device/element used for digital data storage.

Capacity is the maximum amount of data that device can store at any given time.

Access time is the amount of time it takes the external device (processor) to read data from the memory or to write date to the memory.

Memory is divided into **words**. A complete word is always written or read during a data exchange operation.

Each word is assigned a unique number called an **address**.

Classification of memory

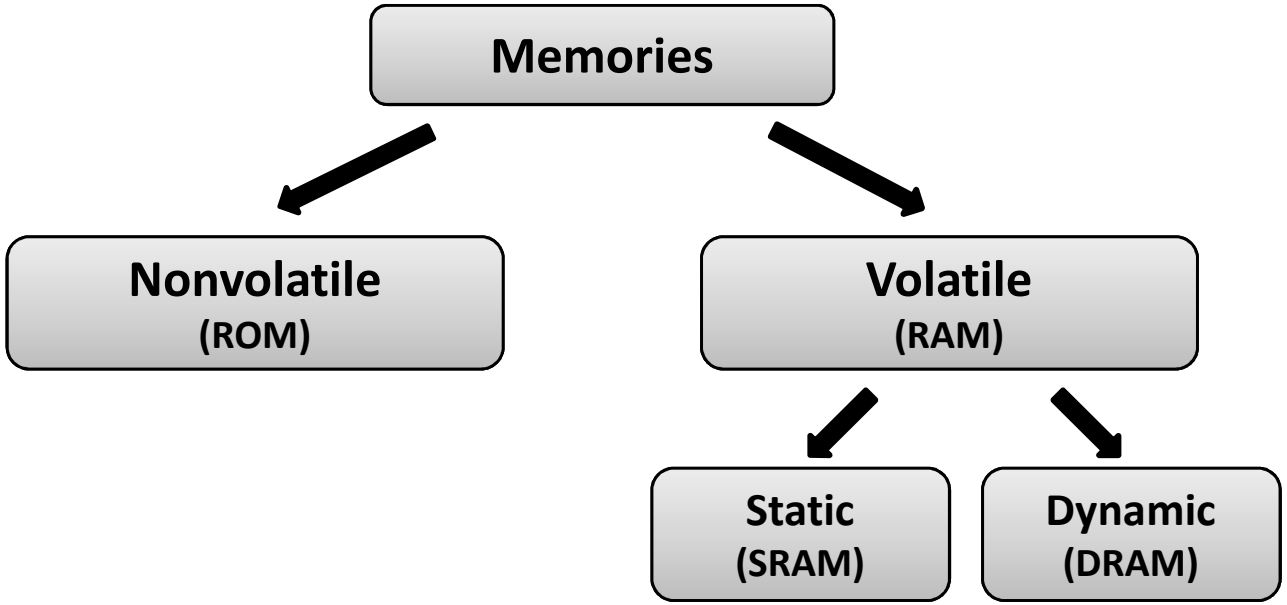
- Nonvolatile (ROM)
- Volatile (RAM)
  - Static (SRAM)
  - Dynamic (DRAM)

- Parallel
- Serial

- Asynchronous
- Synchronous

- Single-port
- Multi-port

Classification of memory (type of memory)



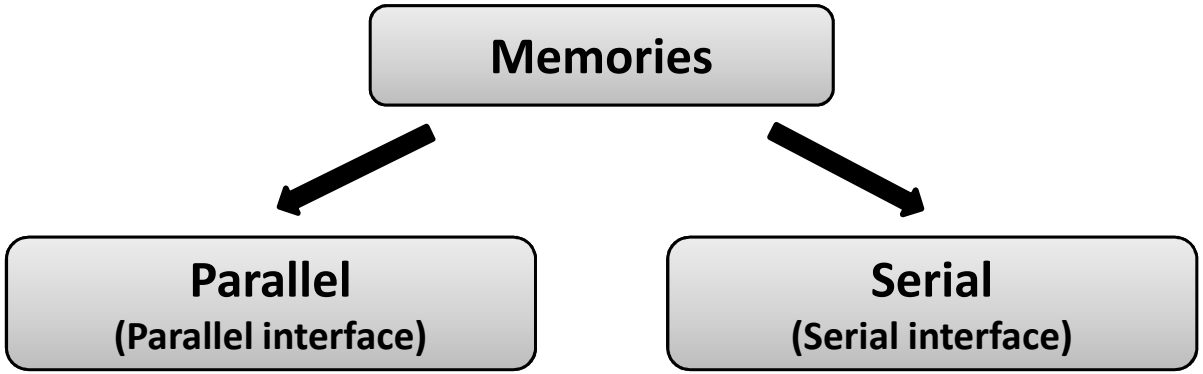
Nonvolatile - ROM (Read Only Memory)
is a type of memory that can retain stored information even after power is removed.
Read-only does not always mean that we cannot write data. It depends on the type of memory. Data stored in ROM cannot be modified (MROM), or can be modified only ones (PROM), or can be modified many times but writing takes place in a different way than reading (EPROM, EEPROM, Flash).

Volatile - RAM (Random Access Memory)
is a type of memory that needs constant power in order to retain data. Data stored in RAM can be modified many times.

SRAM (Static Random Access Memory)
is a type of memory that retains data as long as power is being supplied, but SRAM does not require refresh.

DRAM (Dynamic Random Access Memory)
is a type of memory that retains data as long as power is being supplied, but DRAM require refresh every few milliseconds. Otherwise, the collected data will be lost.

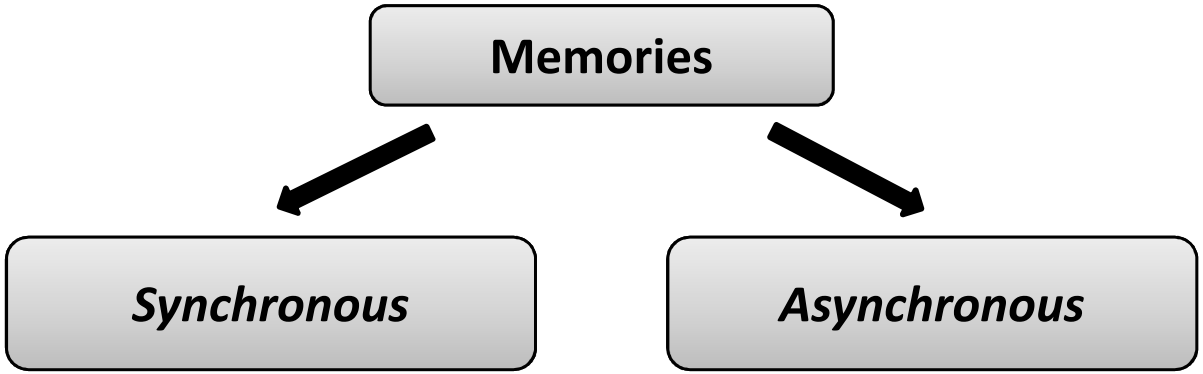
Classification of memory (type of interface)



Memory with parallel interface - require multiple signal lines to communicate. The main advantage is fast transmission (wide data and address buses). The main disadvantage is multiple signals that need to be connected between the memory and external device (processor).

Memory with serial interface - communication is realized via one of the low level protocols (SPI, I2C or 1-Wire). The main advantage is small number of required signals (only 1 to 4 lines). The main disadvantage is low data transfer. In most cases they are used as auxiliary memories (e.g. to store device parameters).

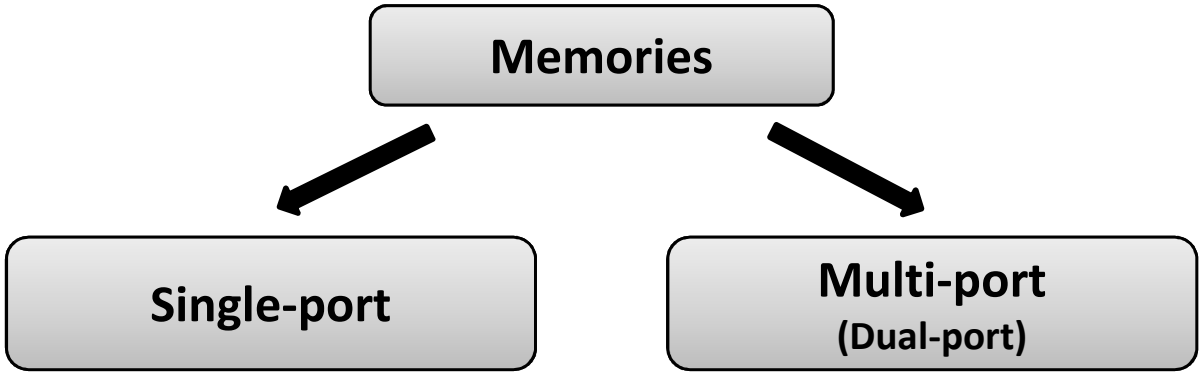
Classification of memory (type of communication)



Synchronous memory - external clock is required. Processor (or other device) need to send the clock signal to communicate. Synchronization with the clock signal causes increase of the baud rate.

Asynchronous memory - the external clock is not required. The transmission signals are not synchronized with the square wave of the clock.

Classification of memory (number of ports)



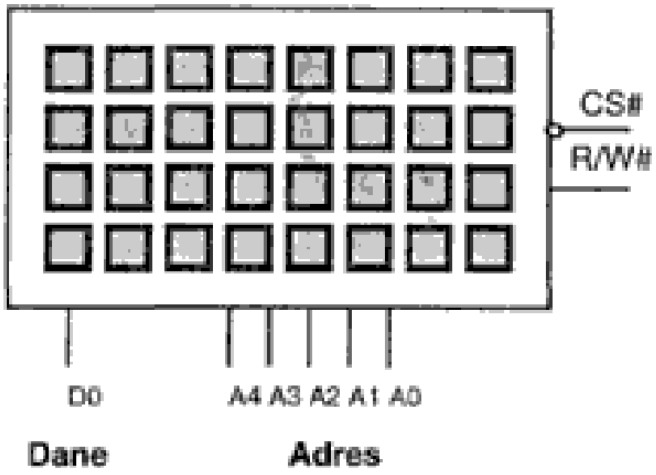
Single-port memory – is a type memory that allows access the memory by only one process, at a time.

Multi-port (Dual-port) memory – is a type memory that allows access the memory by two (or more) processes, at the same time. The multiple-port memories have a few separate interfaces (address buses, data buses, and control lines). The main problem in this kind of memory is simultaneous access to the same data, at the same time.

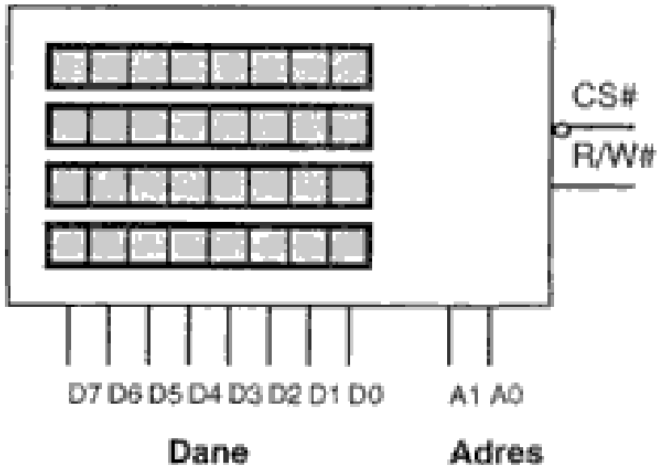
Memory organization

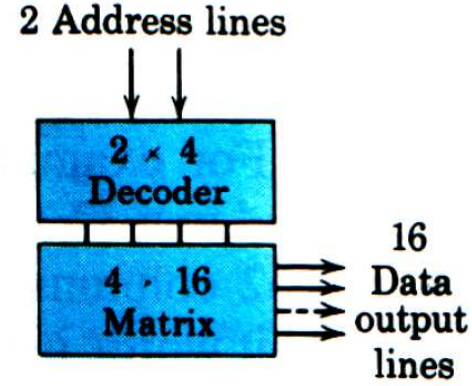
Two-dimensional matrix: column x row

Bit organization
32 x 1 bit

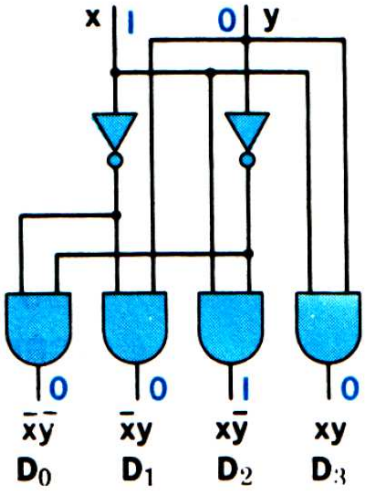


Byte organization
4 x 8 bits





(b) Typical 4 × 16 ROM



(c) 2 × 4 decoder

The way in which memory is divided into words (number of words and words length) is called **memory organization**.

ROM
(Read Only Memory)

Nonvolatile (ROM) is a type of memory that can retain stored information even after power is removed.

Classification of ROM:

- **MROM (Mask ROM)**
- **PROM (Programmable ROM)**
- **EPROM (Erasable Programmable ROM)**
- **EEPROM (Electrically Erasable and Programmable ROM)**
- **FLASH**

Read Only Memories
MROM

MROM *(Mask ROM)* - the memory content is burned onto the chip during the design phase of the semiconductor manufacturing process. User cannot change the content of this memory. MROM is used in systems to store data that do not change - e.g. tables of constants or tables of fonts in displays. In high volumes, Mask Read-Only Memory is a cost-effective alternative to the other type of memories.

Read Only Memories
PROM

PROM (*Programmable ROM*) – is a memory that can be programmed once after it is created. Once the PROM is programmed, the information written is permanent and cannot be deleted. When the PROM is created, all bits read as "1." During the programming, any bit needing to be changed to a "0" is burned into the chip using a special programmer.

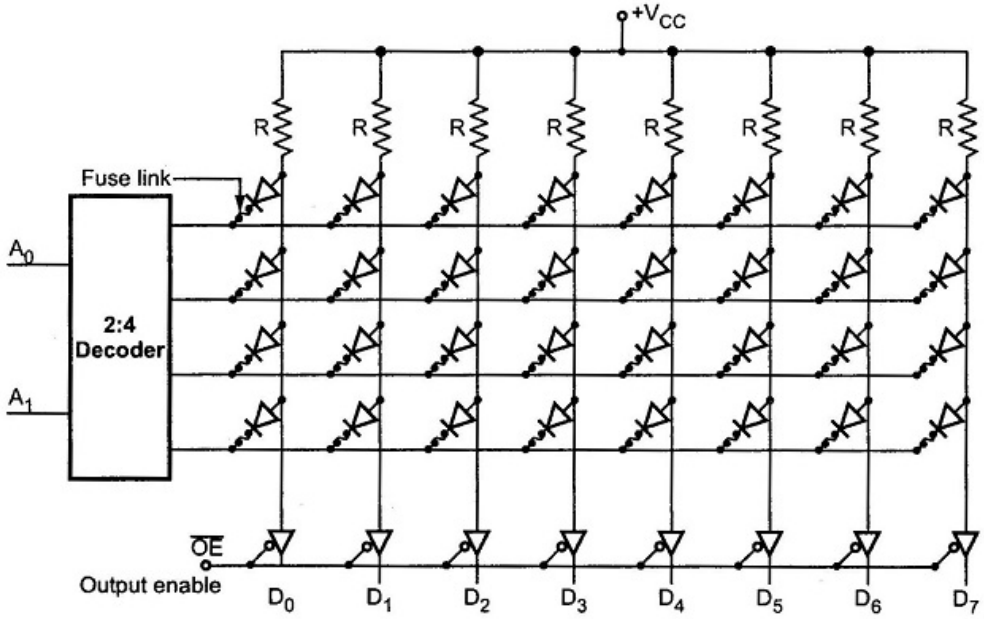
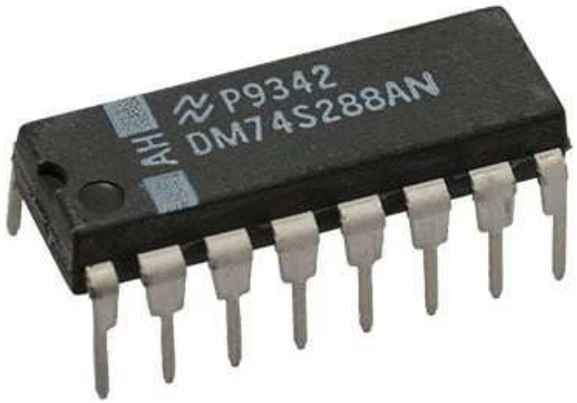
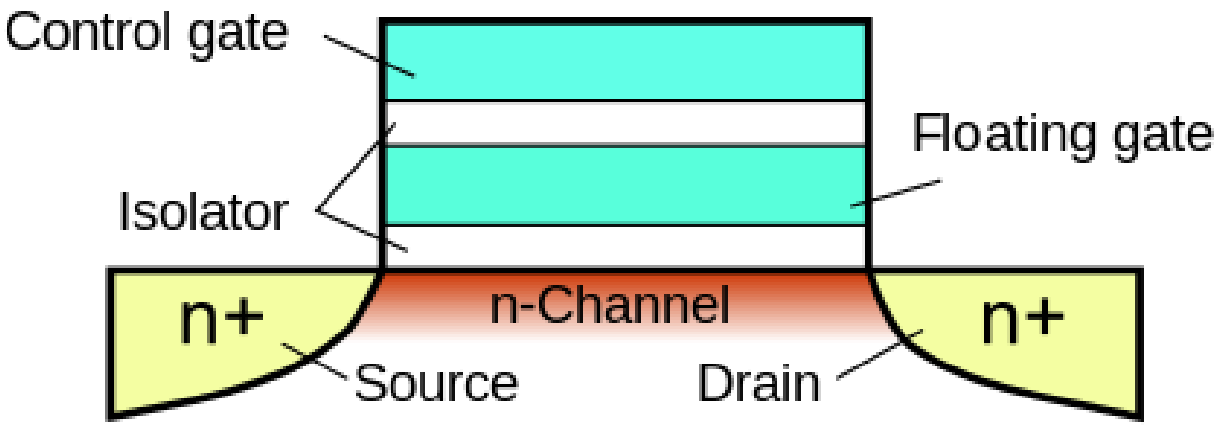


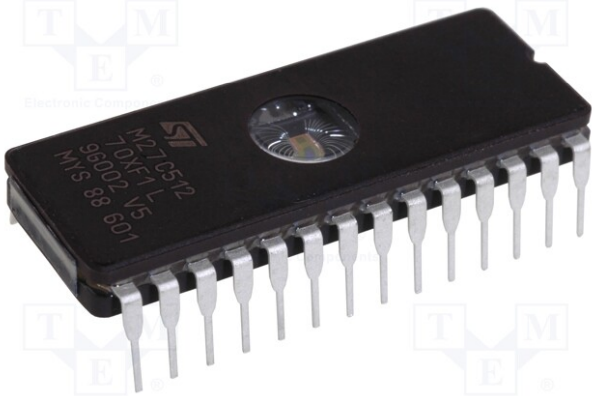
Fig. 3.71 Four byte PROM



Read Only Memories
EPROM

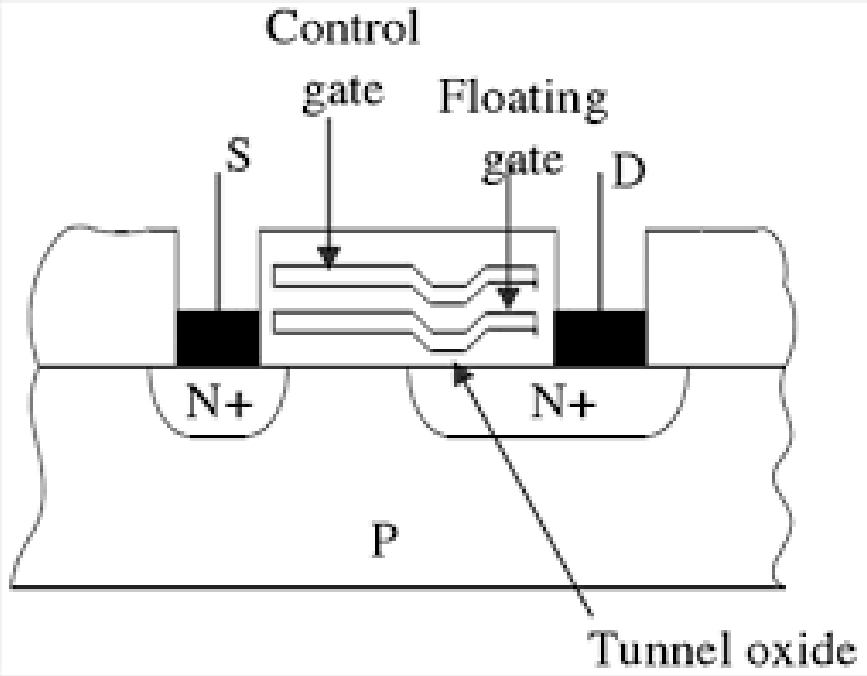
EPROM *(Erasable Programmable ROM)* - the cell of this memory is made of special field-effect transistors with two gates - the control gate, which is normally connected to the memory control signals, and the floating gate, which is not connected. Both of these gates are separated from each other by an insulator. Thanks to the quantum phenomenon of electron tunneling, a floating gate can accept electrons by simply applying a higher voltage to the control gate. The electrons collected in the floating gate create a negative electric field, which prevents the transistor from conducting. Lack of conduction is identified as logic state 0, conducts is identified as the logical state 1. Content of this memory can be removed by exposing the silicon structure to ultraviolet light.





Read Only Memories
EEPROM

EEPROM (*Electrically Erasable and Programmable ROM*) - the memory cell in this kind of memory is very similar to the previous memory (EPROM). The main difference is using of a different insulator. It allows to enables the electron tunneling phenomena in the way of electric control. Because we have purely electrical programming and erasing, EEPROM memories can be programmed directly in a digital system.

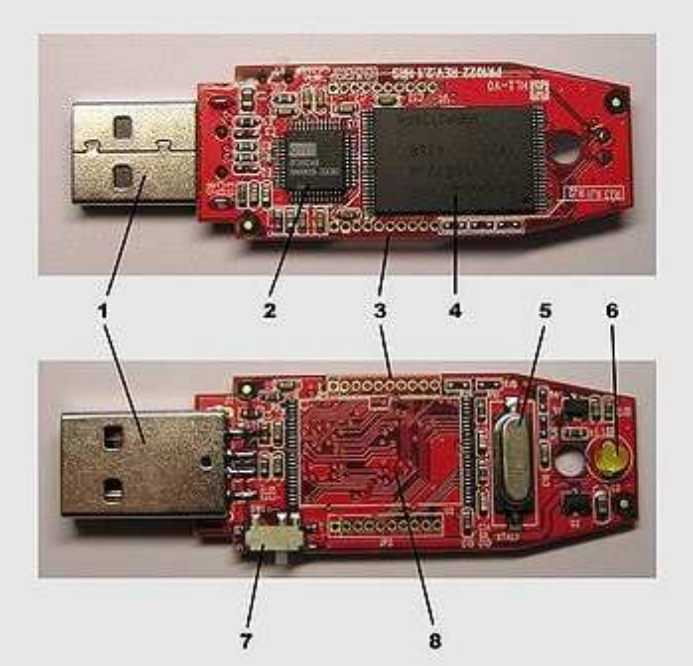


Read Only Memories
FLASH

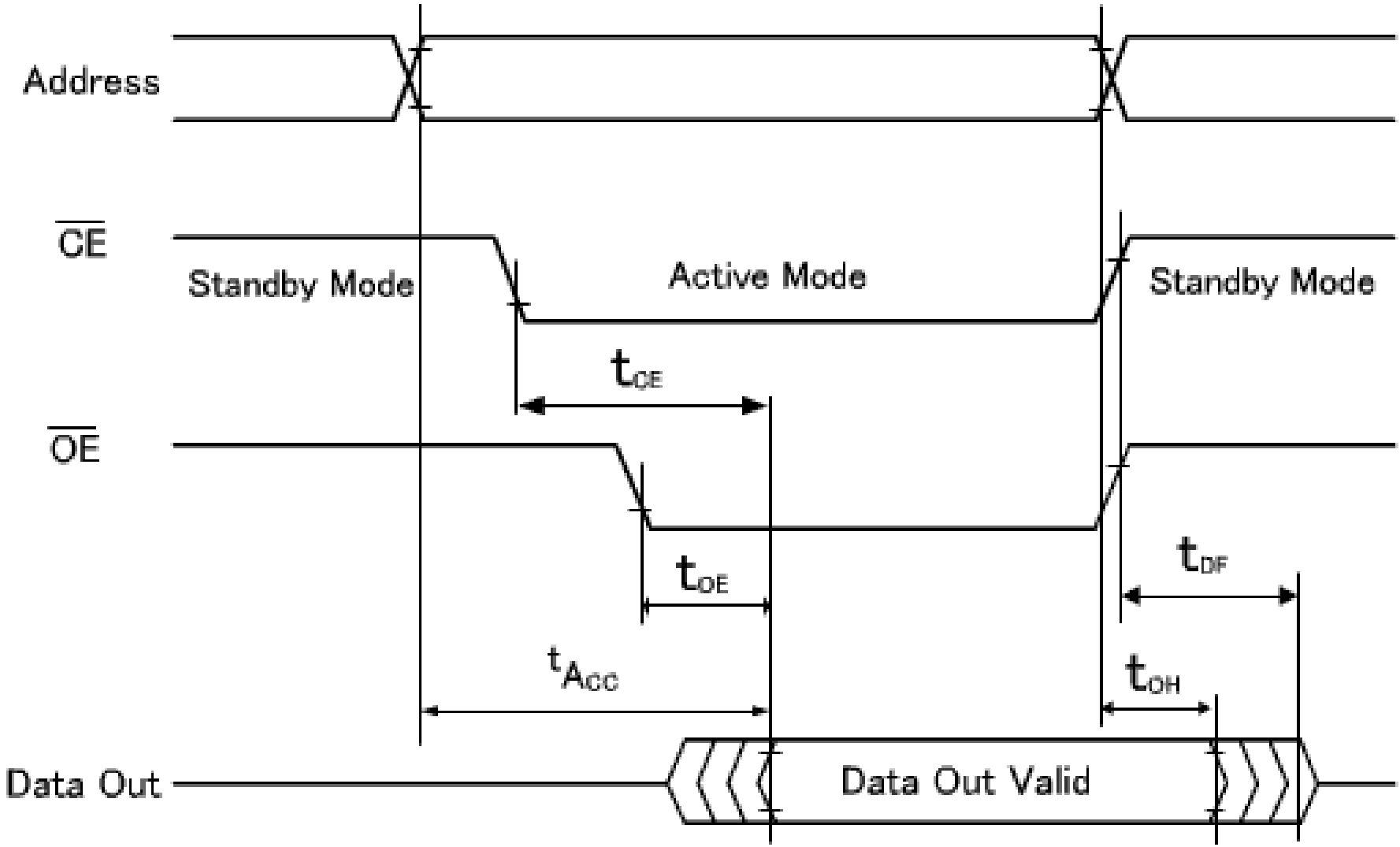
FLASH - Flash is a specific type of EEPROM memory. The structure of this memory is the same like in the EEPROM. The main difference occurs for delete a stored information. In case of the standard EEPROM only single cells (only a single words) is deleted. But in the flash memory the entire block of cells (usually one thousand bytes) is deleted. For this reason, at the same time many words can be erased from the FLASH memory. Deleting entire blocks is very beneficial, because usually data in digital systems (like computer) are organized in the form of data blocks.

Flash memories are available in two technologies, based on NOR or NAND gates. Memories based on the NOR gates allows to fast reading but slow writing and erasing.

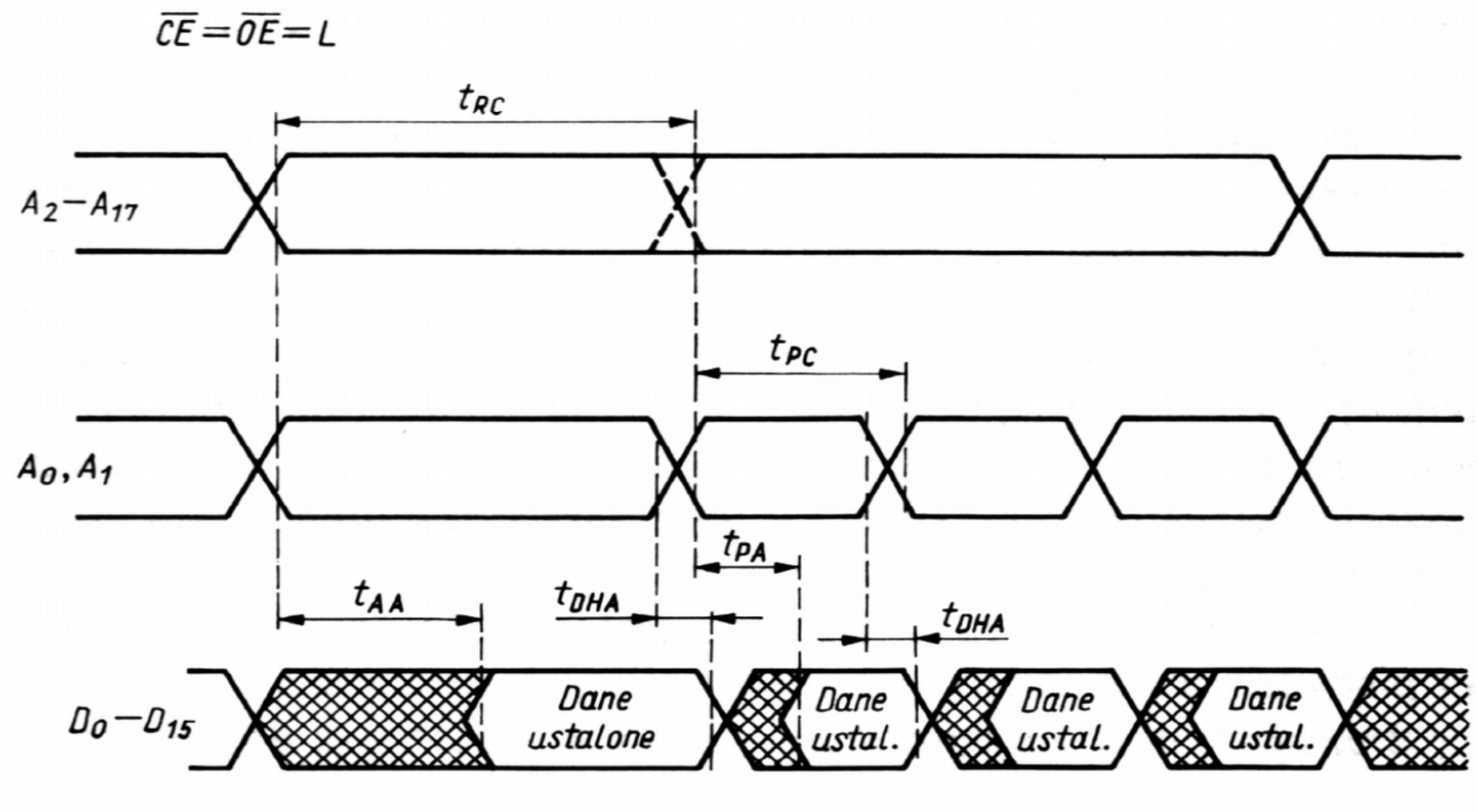
Memories based on the NAND gates allows to quick save and erase. There are cheaper to produce (in comparison with NOR technology), and there are used in mass memories.



Read Only Memories
Read timing



Read Only Memories
Burst read (asynchronous reading of the series)



RAM
(Random Access Memory)

Volatile (RAM) is a type of memory that needs constant power in order to retain data. Data stored in RAM can be modified many times.

Classification of RAM:

- ***Static RAM***
- ***Synchronous Static RAM***
- ***Dynamic RAM***
- ***Synchronous Dynamic RAM***
- ***Double Data Rate SDRAM***

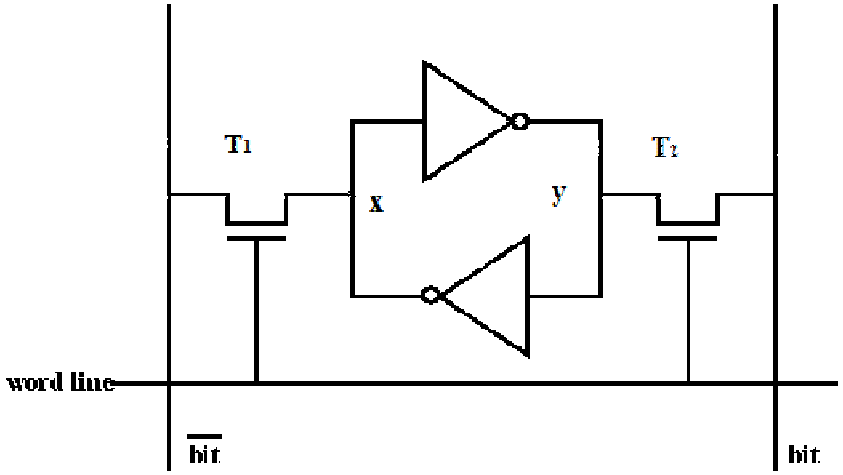
Static RAM

SRAM (Static RAM) – is a type of volatile memory that retains data as long as power is being supplied, but SRAM does not require refresh. Unlike Dynamic RAM (DRAM), which must be periodically refreshed.

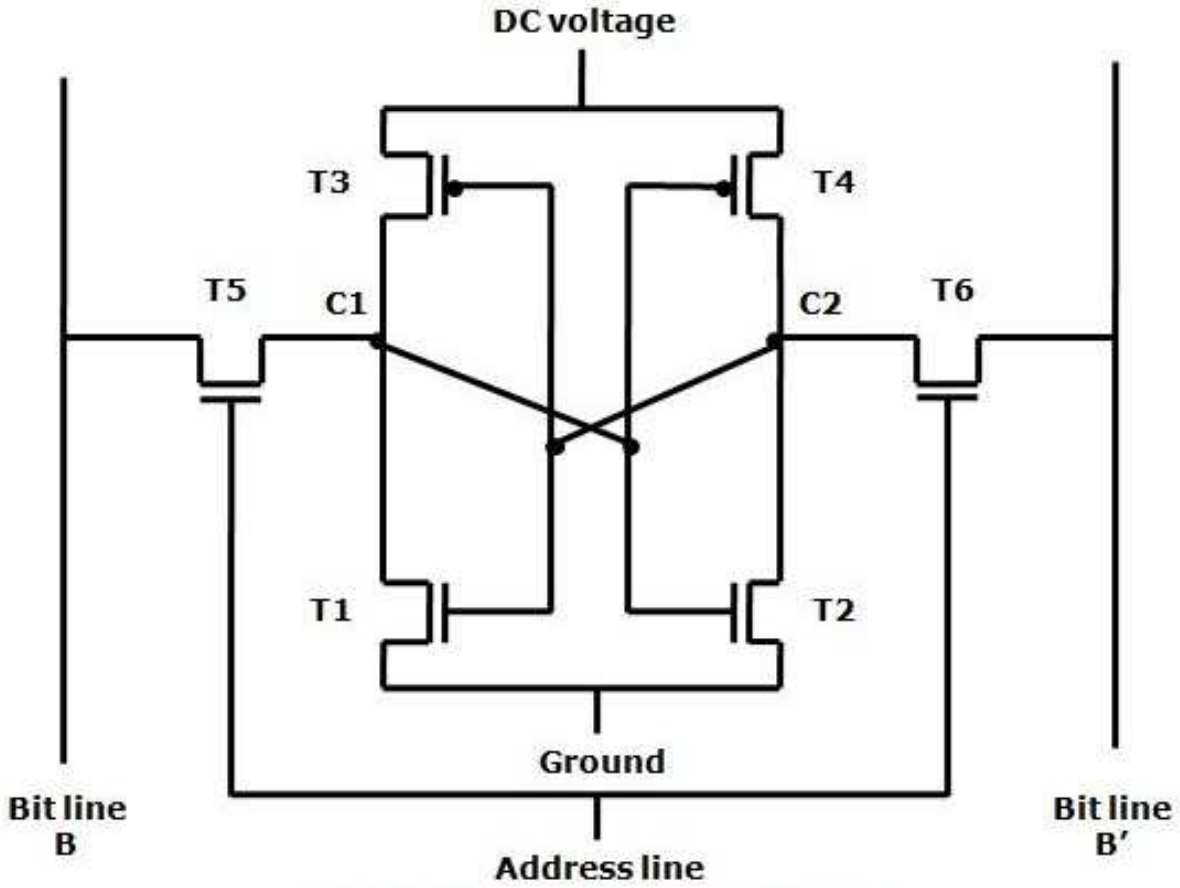
Main features of Static RAM:

- very fast kind of memory;
- difficult to integrate;
- commonly used for a computer's cache memory;
- it is not used for a computer's main memory because of its cost and size;
- Static RAM might be part of:
  - ADC converter memory,
  - on a computer's graphic card,
  - in a disk drive as buffer cache,
  - in a peripheral such as a printer or LCD display,
  - in a network device such as router or switch.

SRAM
Cell structure



Simplified structure of the SRAM cell.

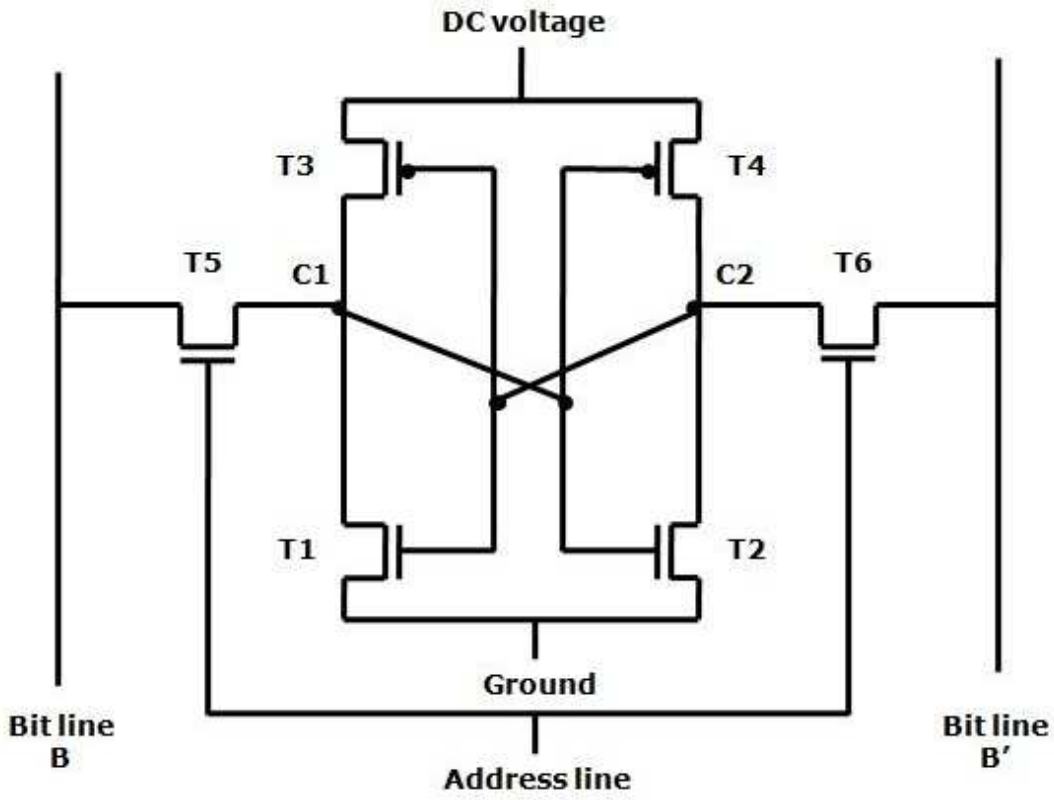


Static RAM (SRAM) Cell

SRAM
States of working

Three states of working:

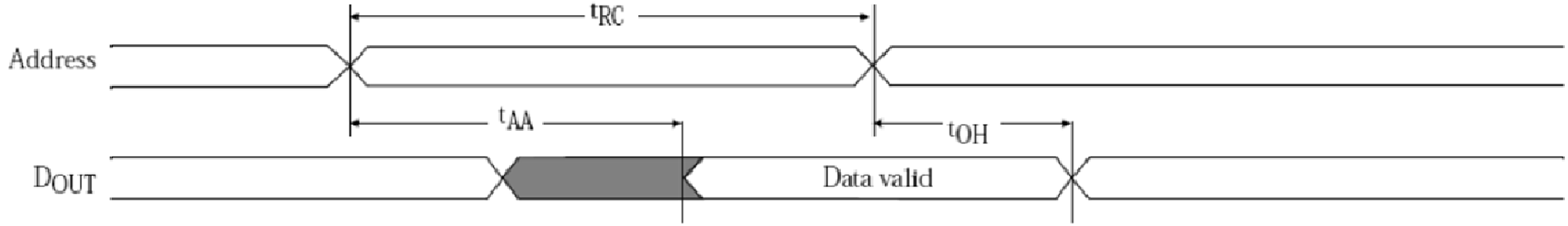
- **IDLE -** the address line is inactive; the two cross-coupled inverters formed from transistors T1-T4 are in one of the two bi-stable states.
- **READ –** the address line is set as active; transistors T5 and T6 cause connection cell to the data lines;
- **WRITE -** the address line is set as active; transistors T5 and T6 cause connection cell to the data lines; due to the fact, that the data line drivers are designed to be much stronger than the relatively weak transistors in the cell, drivers force a state change in the cell; after a change of state, the flip-flop remembers the new value of the data.



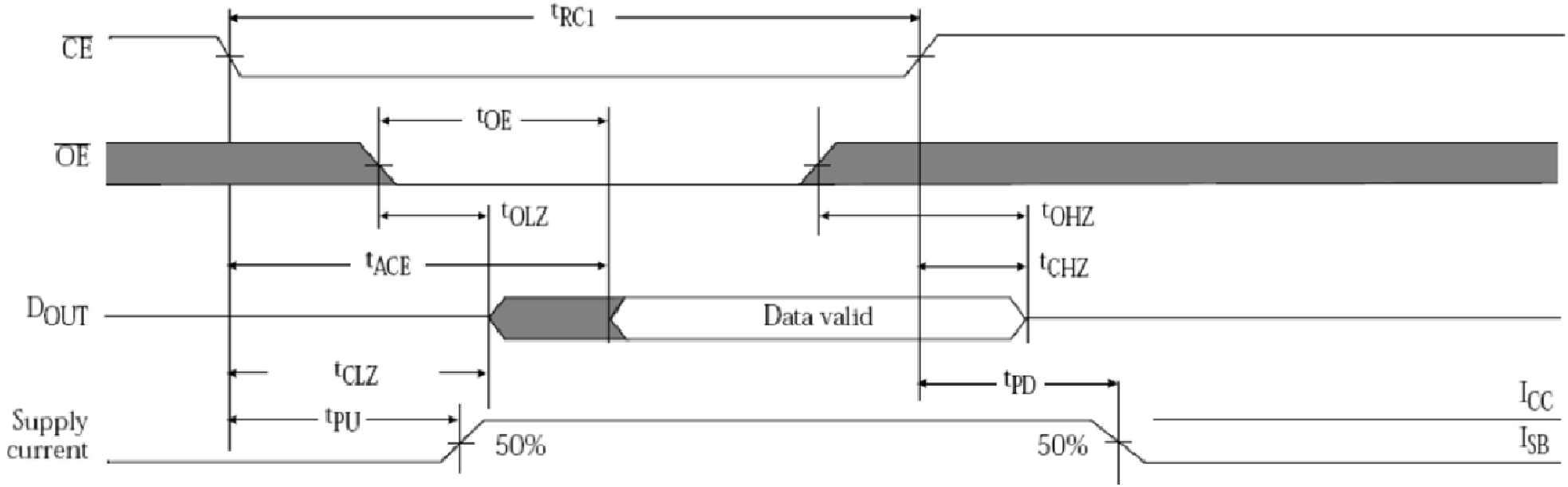
Static RAM (SRAM) Cell

Asynchronous SRAM
Read timing

Read waveform 1 (address controlled)

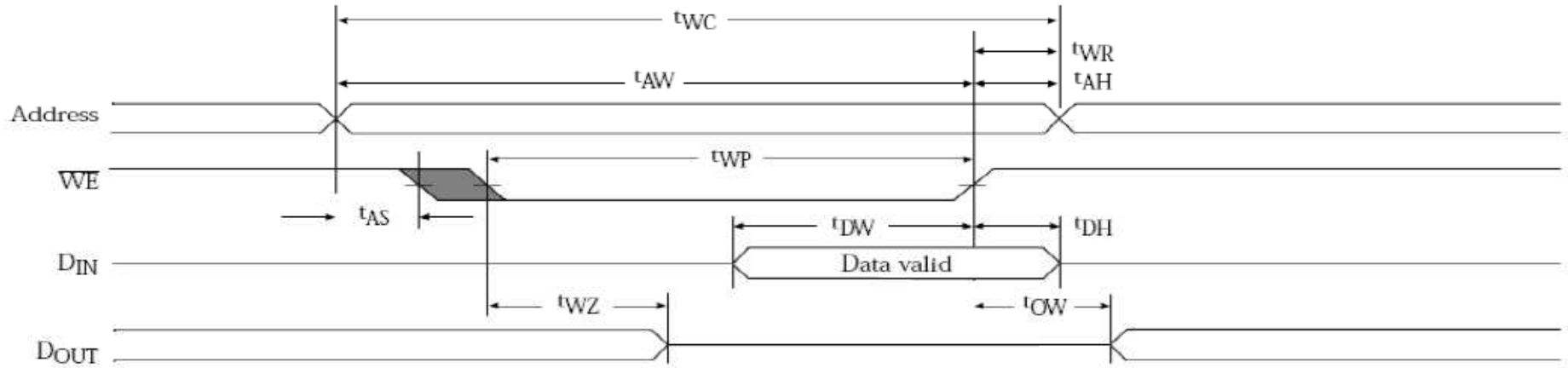


Read waveform 2 ($\overline{CE}$, $\overline{OE}$ controlled)

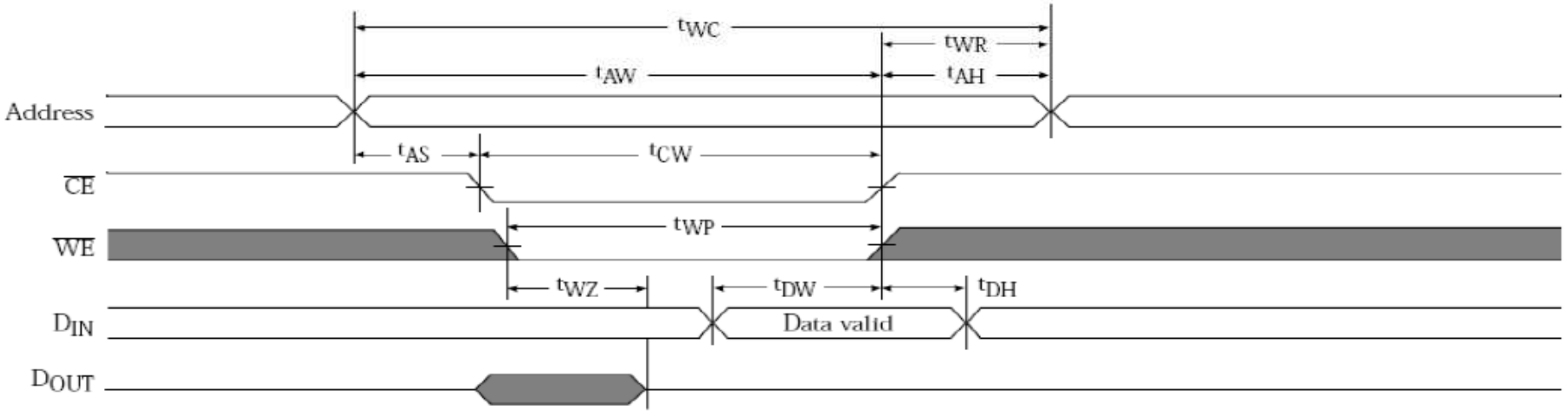


Asynchronous SRAM
Write timing

Write waveform 1 ($\overline{WE}$ controlled)



Write waveform 2 ($\overline{CE}$ controlled)

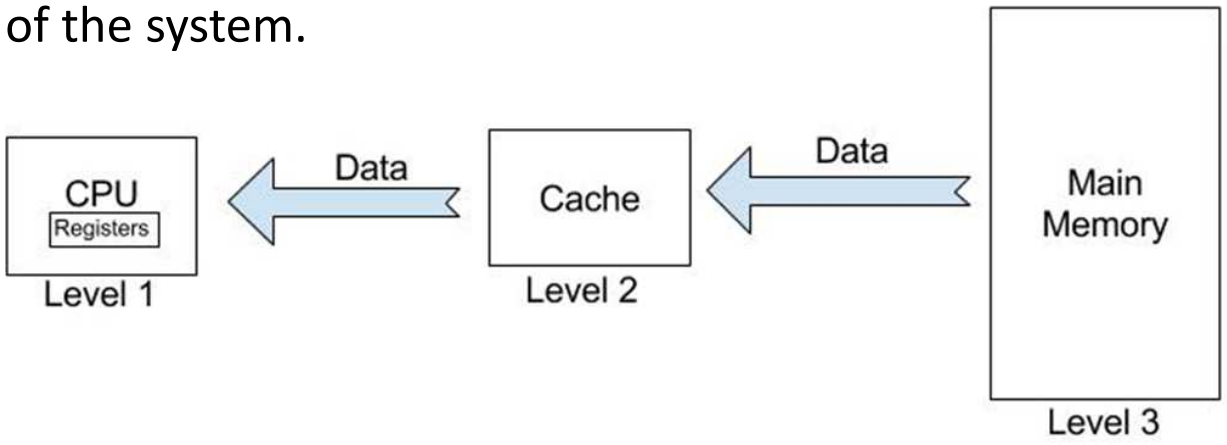


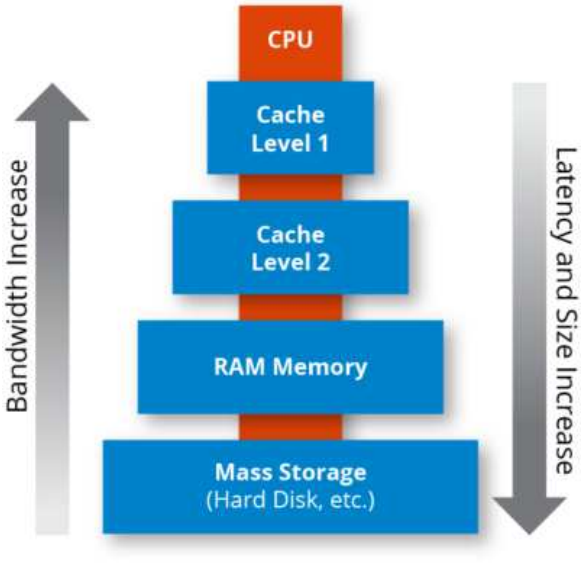
SSRAM

SSRAM (Synchronous Static RAM) – is type of memory that are synchronized with an external clock signal. SSRAM will read and write information into the memory only on particular states of the clock (on the edges). The structure of this type of memory is very similar to asynchronous SRAM.

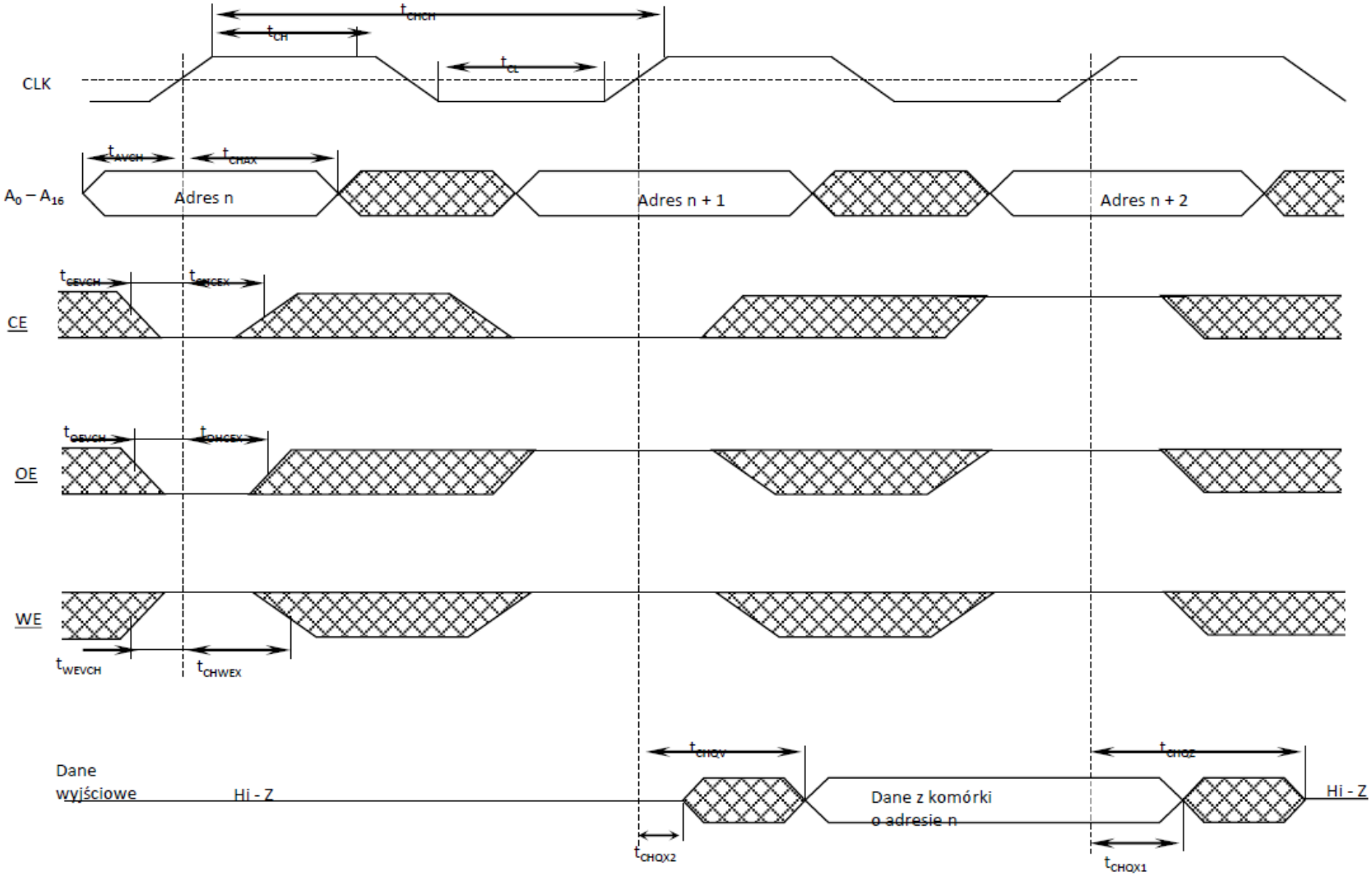
The most common application for SSRAM is Cache memory, which is used to supply a processor with the most frequently requested instructions and data. Instructions and data located in cache memory can be accessed many times faster than instructions and data located in main memory (typically SDRAM).

The more instructions and data a processor can access directly from cache memory, the better overall performance of the system.

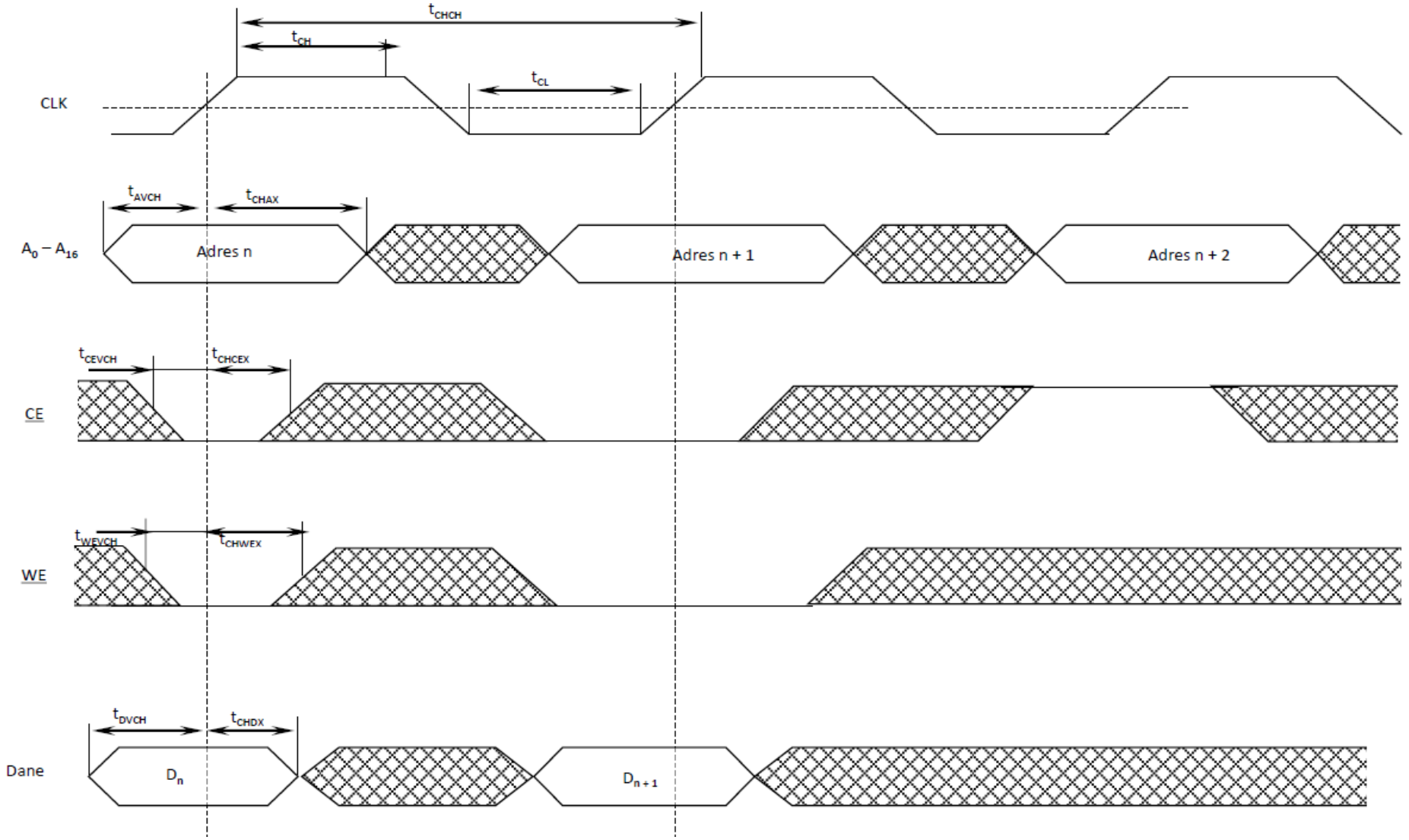




Synchronous Static RAM (SSRAM)
Read timing



Synchronous Static RAM (SSRAM)
Write timing

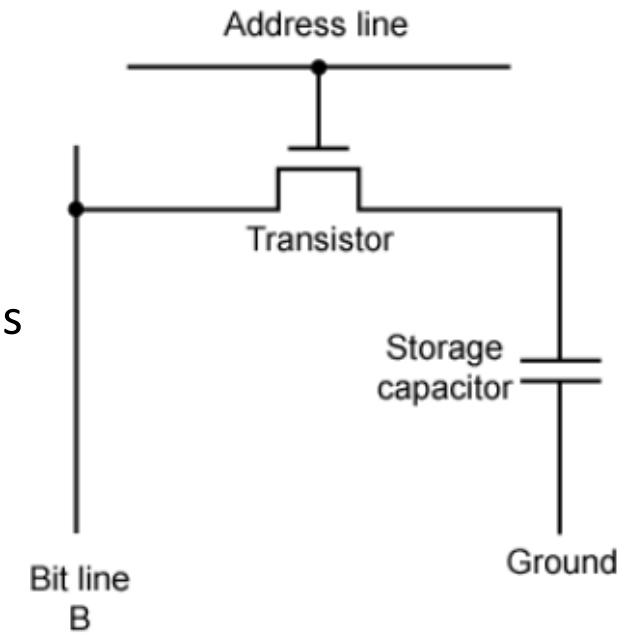


DRAM
Cell structure

DRAM (Dynamic RAM) – is a type of memory that retains data as long as power is being supplied, but DRAM require refresh every few milliseconds. Otherwise, the collected data will be lost. The refresh cycle should occur approximately every 8-20 ms. **Information is stored in the form of an electric charge.**

Write operation

- the voltage on the bit line is given - high for 1 and low for 0;
- control signal is given to the address line;
- a current flows which charges/discharges the capacitor.

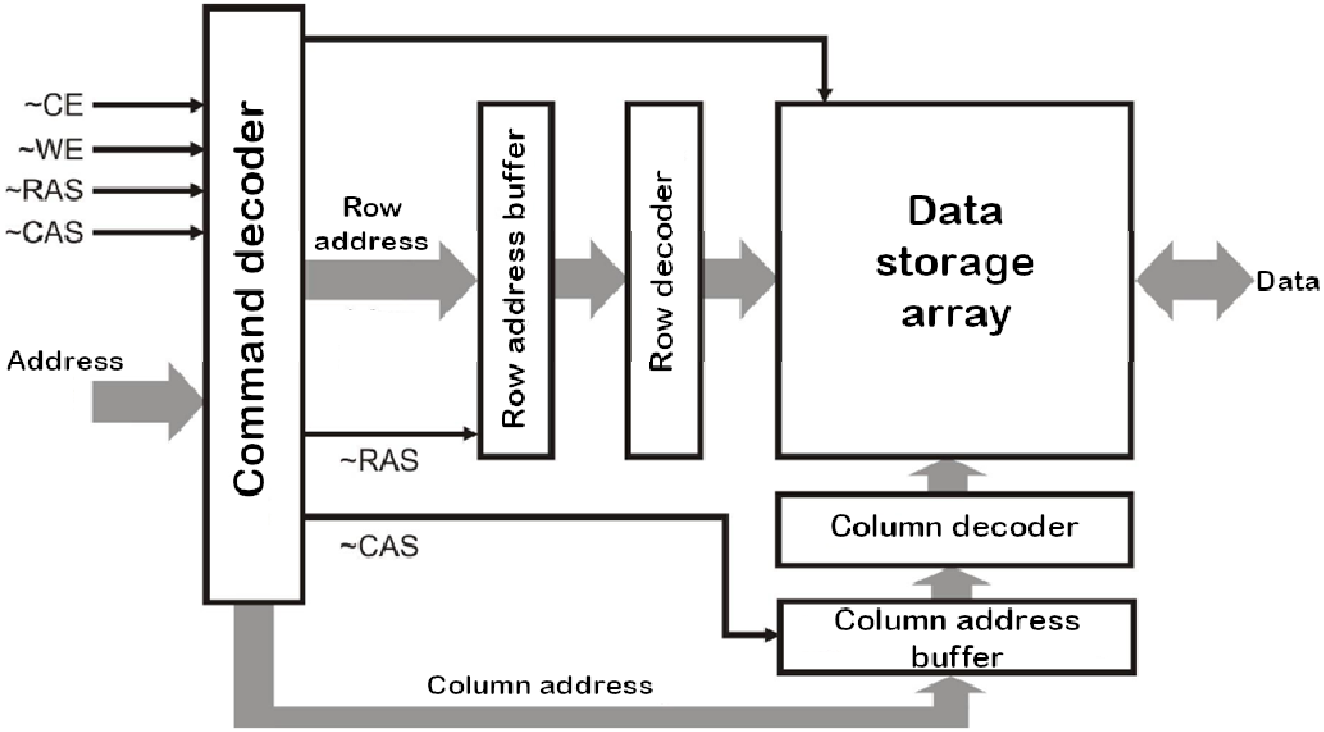


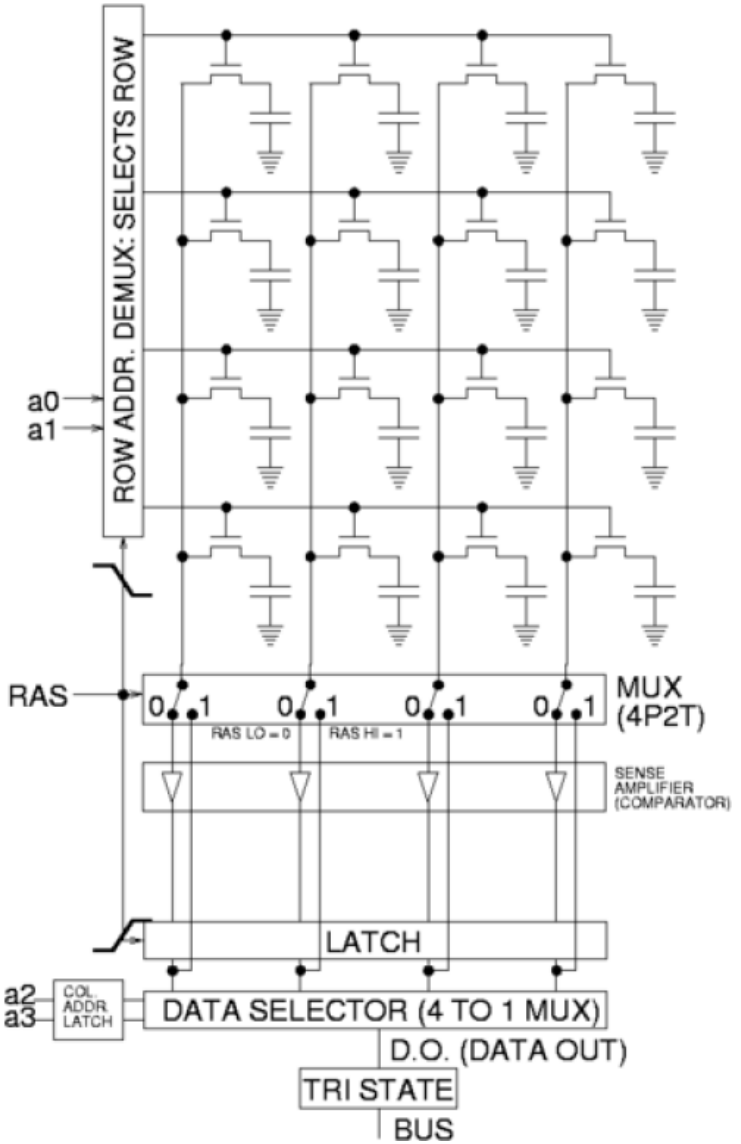
Read operation

- the signal is given to the address line - the transistor channel is opened;
- the capacitor discharges through the bit line to the sensor;
- follows comparison the read voltage with the pattern to determine the value of the bit (0 or 1);
- the state of charge of the capacitor is restored.

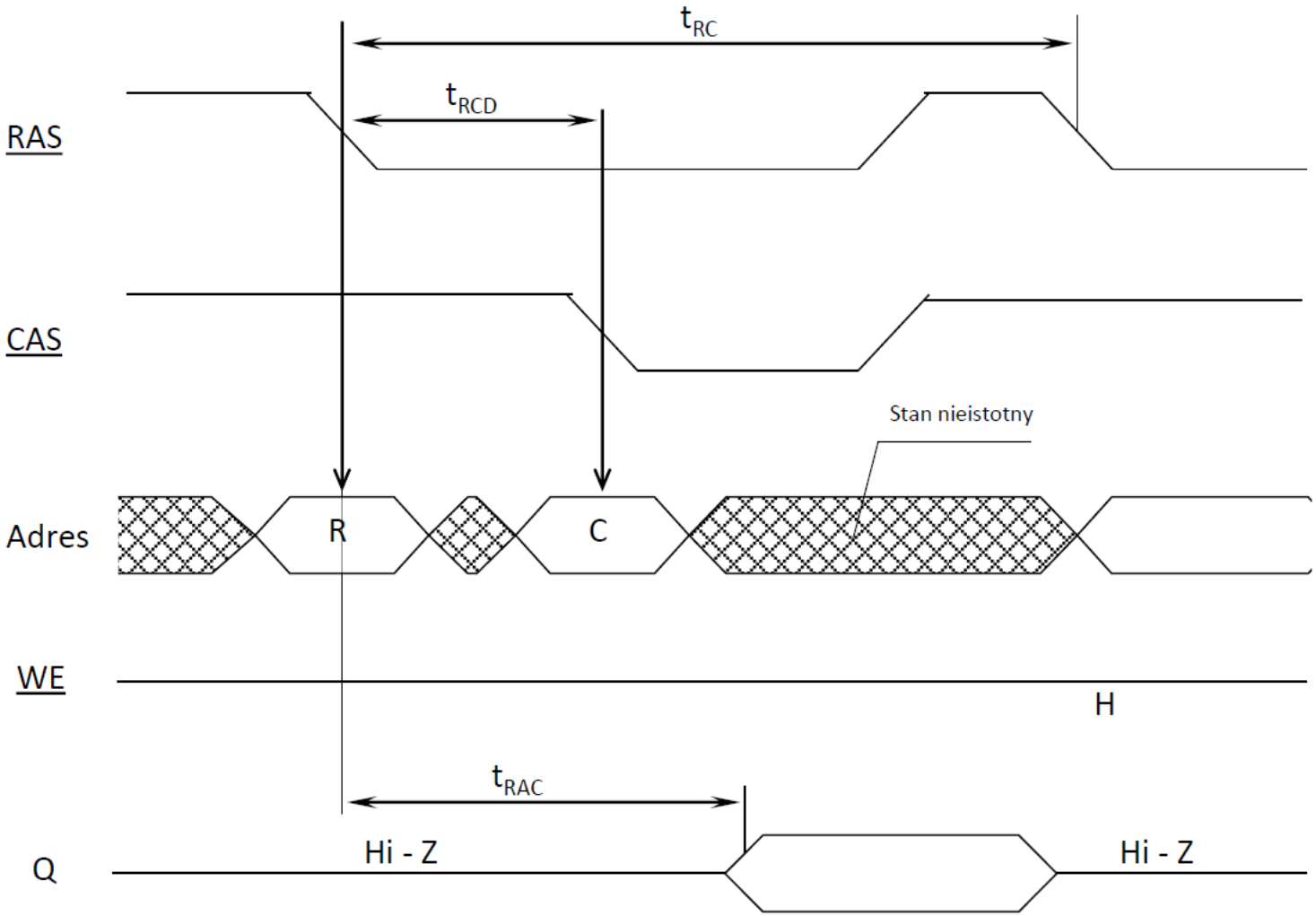
DRAM
Memory architecture

The address is given in two steps:
~RAS - Row Address Strobe
~CAS - Column Address Strobe





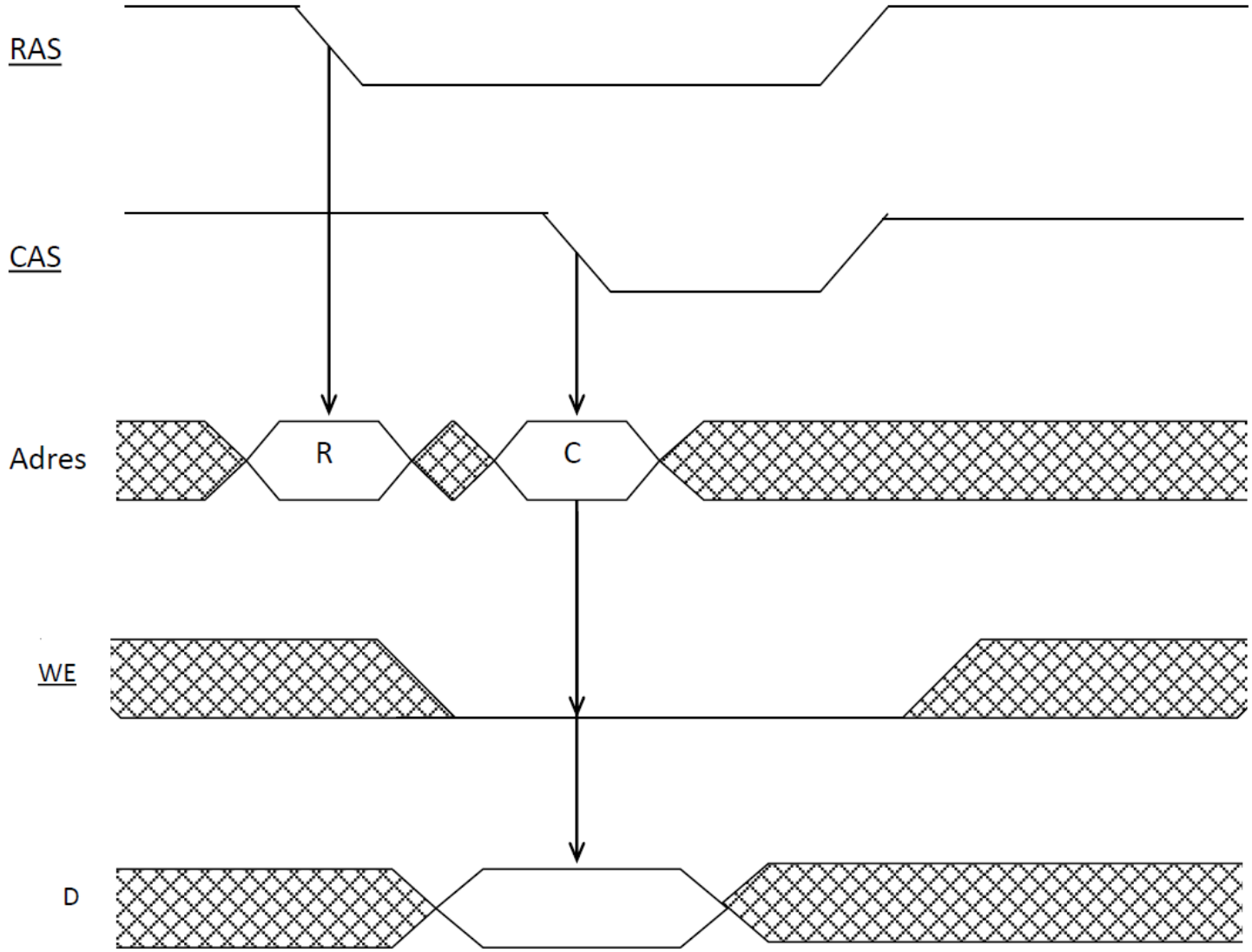
DRAM
Read timing



RAS – Row Address Strobe

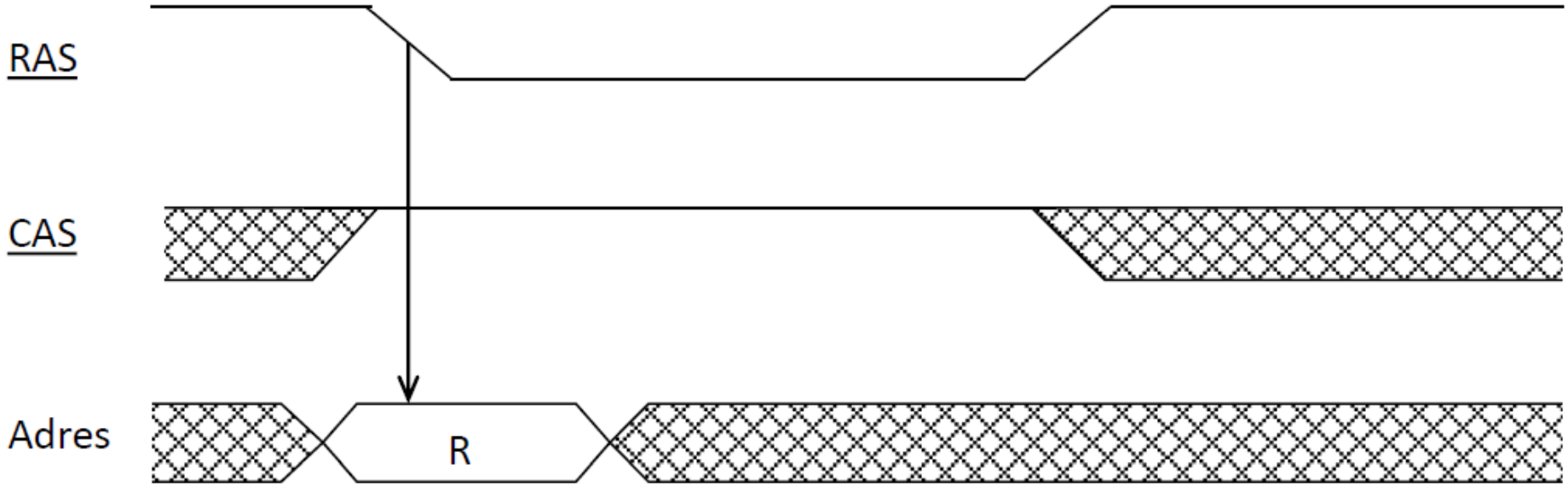
CAS – Column Address Strobe

DRAM
Write timing



DRAM
Refreshing

- **Normal refreshing – refreshing the entire row**



- **/CAS before /RAS -** if CAS negated signal is set low before the RAS negated signal, the DRAM memory ignores the address given on the address bus and uses its internal counter to refresh the next line.

SDRAM

SDRAM (Synchronous Dynamic Random Access Memory) - is the name for memory where the operation the external interface is synchronized by an external clock signal. Traditional forms of memory including DRAM operate in an asynchronous manner. SDRAM is able to operate more efficiently. It is synchronized to the clock of the processor and hence to the bus. This enables it to operate at much higher speeds.

- All SDRAM control signals are synchronized with one clock waveform. This makes it easier for the memory to work with other devices.

- The timing signal synchronization with the clock allows to accelerate the operation of the memory.

- Refresh of the cells are realized by internal refresh generator. Thus, external controller (in processor) does not need to carry out this operation. For this reason the transmission speed can be increased.

DDR SDRAM

DDR (Double Data Rate SDRAM) is the next generation following SDRAM. DDR transfers data to the processor **on both the rising and falling edges of the clock signal**, so twice per cycle. Using both edges to transfer data makes DDR memory significantly faster than SDRAM, which uses only one edge of the clock signal to transfer data.

- DDR use both edges to transfer data.
- The supply voltage has been reduced from 3.3V to 2.5V.
- Transmission speed: 2 x 64 (bus width) x f (clock frequency) [B/s].

Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	Module name	Peak transfer rate
DDR-200	100 MHz	10 ns [1]	100 MHz	200 Million	PC-1600	1600 MB/s
DDR-266	133 MHz	7.5 ns	133 MHz	266 Million	PC-2100	2100 MB/s
DDR-300	150 MHz	6.67 ns	150 MHz	300 Million	PC-2400	2400 MB/s
DDR-333	166 MHz	6 ns	166 MHz	333 Million	PC-2700	2700 MB/s
DDR-400	200 MHz	5 ns	200 MHz	400 Million	PC-3200	3200 MB/s
DDR-500	250 MHz	4 ns	250 MHz	500 Million	PC-4000	4000 MB/s
*DDR-650	325 MHz	3.1 ns	325 MHz	650 Million	PC-5200	5200 MB/s

DDR2 SDRAM

DDR2 - uses the same internal clock speed as DDR, however, the transfer rates are faster due to the increased size of the data buffer.

- DDR2 use both edges to transfer data.
- The internal memory frequency is 2 times lower than the external bus frequency - therefore, during one reading, 4 bits are read from the internal memory, which are transferred one by one. The prefetch buffer of DDR2 is 4 bits (double of DDR).
- Reduced supply voltage to 1.8V.
- Increased external data bus clock - twice as fast as DDR.

Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	Module name	Peak transfer rate
DDR2-400	100 MHz	10 ns	200 MHz	400 Million	PC2-3200	3200 MB/s
DDR2-533	133 MHz	7.5 ns	266 MHz	533 Million	PC2-4200 PC2-4300[1]	4266 MB/s
DDR2-667	166 MHz	6 ns	333 MHz	667 Million	PC2-5300 PC2-5400[1]	5333 MB/s
DDR2-800	200 MHz	5 ns	400 MHz	800 Million	PC2-6400	6400 MB/s
DDR2-1066	266 MHz	3.75 ns	533 MHz	1066 Million	PC2-8500 PC2-8600[1]	8533 MB/s
DDR2-1300	325 MHz	3.1 ns	650 MHz	1300 Million	PC2-10400	10400 MB/s

DDR3 SDRAM

- DDR3 use both edges to transfer data.
- The internal memory frequency is 4 times lower than the external bus frequency - therefore, during one reading, 8 bits are read from the internal memory, which are transferred one by one. The prefetch buffer of DDR3 is 8 bits (double of DDR2).
- Reduced supply voltage to 1.5V.
- Significant reduction in power consumption – roughly 40% compared to DDR2.
- DDR3 also adds functions that the memory control the refresh rate according to the temperature variation.

Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	Module name	Peak transfer rate
DDR3-800	100 MHz	10 ns	400 MHz	800 Million	PC3-6400	6400 MB/s
DDR3-1066	133 MHz	7.5 ns	533 MHz	1066 Million	PC3-8500	8533 MB/s
DDR3-1333	166 MHz	6 ns	667 MHz	1333 Million	PC3-10600	10667 MB/s[1]
DDR3-1600	200 MHz	5 ns	800 MHz	1600 Million	PC3-12800	12800 MB/s

Summary
DDRx comparison

DDR2 – DDR4 evolved to require lower supply voltages, which generally saves power. Other changes were made to increase the speed, as well. DDR2 was reduced to operating at a voltage of 1.8 volts, and a clock multiplier was added to the memory module to again double data transfer speeds while operating at the same bus speed. DDR3 integrated a 4x clock multiplier, again doubling the memory transfer rate for the same bus speed.

	DRAM	DDR	DDR2	DDR3	DDR4	DDR5
Prefetch	1 – Bit	2 - Bit	4 - Bit	8 - Bit	Bit per Bank	16 - Bit
Data Rate (MT/s)	100 - 166	266 - 400	533 - 800	1066 - 1600	2133 - 5100	3200 - 6400
Transfer Rate (GB/s)	0.8 - 1.3	2.1 - 3.2	4.2 - 6.4	8.5 - 14.9	17 - 25.6	38.4 - 51.2
Voltage (V)	3.3	2.5 - 2.6	1.8	1.35 - 1.5	1.2	1.1

Summary
Static RAM and Dynamic RAM comparison

Static RAM	Dynamic RAM
➢ SRAM uses transistor to store a single bit of data	➢ DRAM uses a separate capacitor to store each bit of data
➢ SRAM does not need periodic refreshment to maintain data	➢ DRAM needs periodic refreshment to maintain the charge in the capacitors for data
➢ SRAM's structure is complex than DRAM	➢ DRAM's structure is simplex than SRAM
➢ SRAM are expensive as compared to DRAM	➢ DRAM's are less expensive as compared to SRAM
➢ SRAM are faster than DRAM	➢ DRAM's are slower than SRAM
➢ SRAM are used in Cache memory	➢ DRAM are used in Main memory

Summary
RAM and ROM comparison

RAM	ROM
1. Temporary Storage.	1. Permanent storage.
2. Store data in MBs.	2. Store data in GBs.
3. Volatile.	3. Non-volatile.
4. Used in normal operations.	4. Used for the startup process of computers.
5. Writing data is faster.	5. Writing data is slower.

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