Actuating, Sensing and Control
Mechatronic Systems

System on Chip

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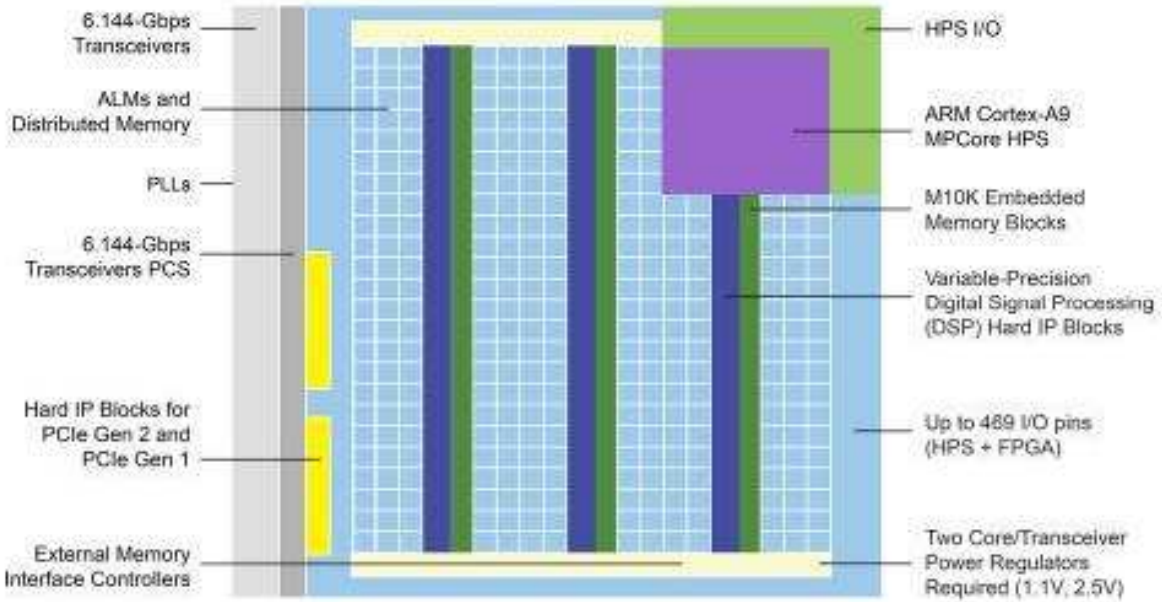
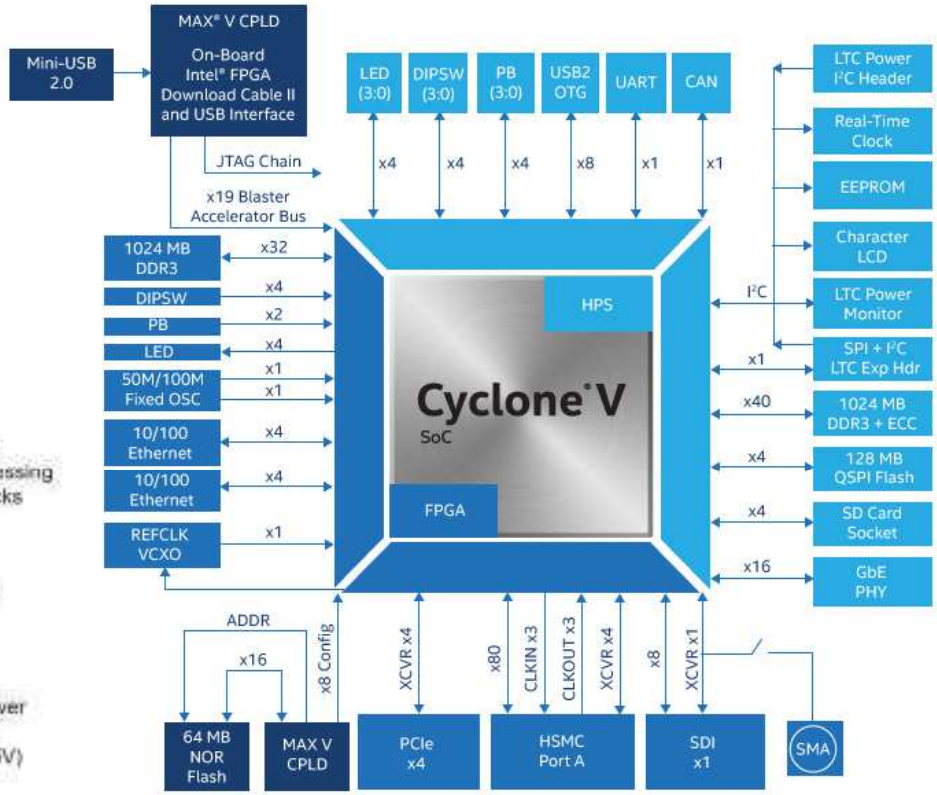
AGENDA

1. SoC = FPGA + HPS (MCU)
2. Power Configurations
3. FPGA and HPS Communications
4. Memory mapping
5. SD Card Image
6. HSP Peripherals
7. HPS Booting Process
8. DE10-Nano

Cyclone V SoC
FPGA + HPS

Cyclone V SoC FPGA devices offer a dual-core Arm Cortex-A9 MPCore processor surrounded by rich peripherals and a hardened memory controller. The FPGA fabric is connected to the hard processor system (HPS) through a high-speed >100Gbps interconnect backbone.





Cyclone V SoC
Possible HPS and FPGA Power Configurations

The HPS and FPGA portions of the device have separate external power supplies and are power on independently. You can power on the HPS without powering on the FPGA side of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion.

HPS Power	FPGA Power
On	On
On	Off
Off	Off

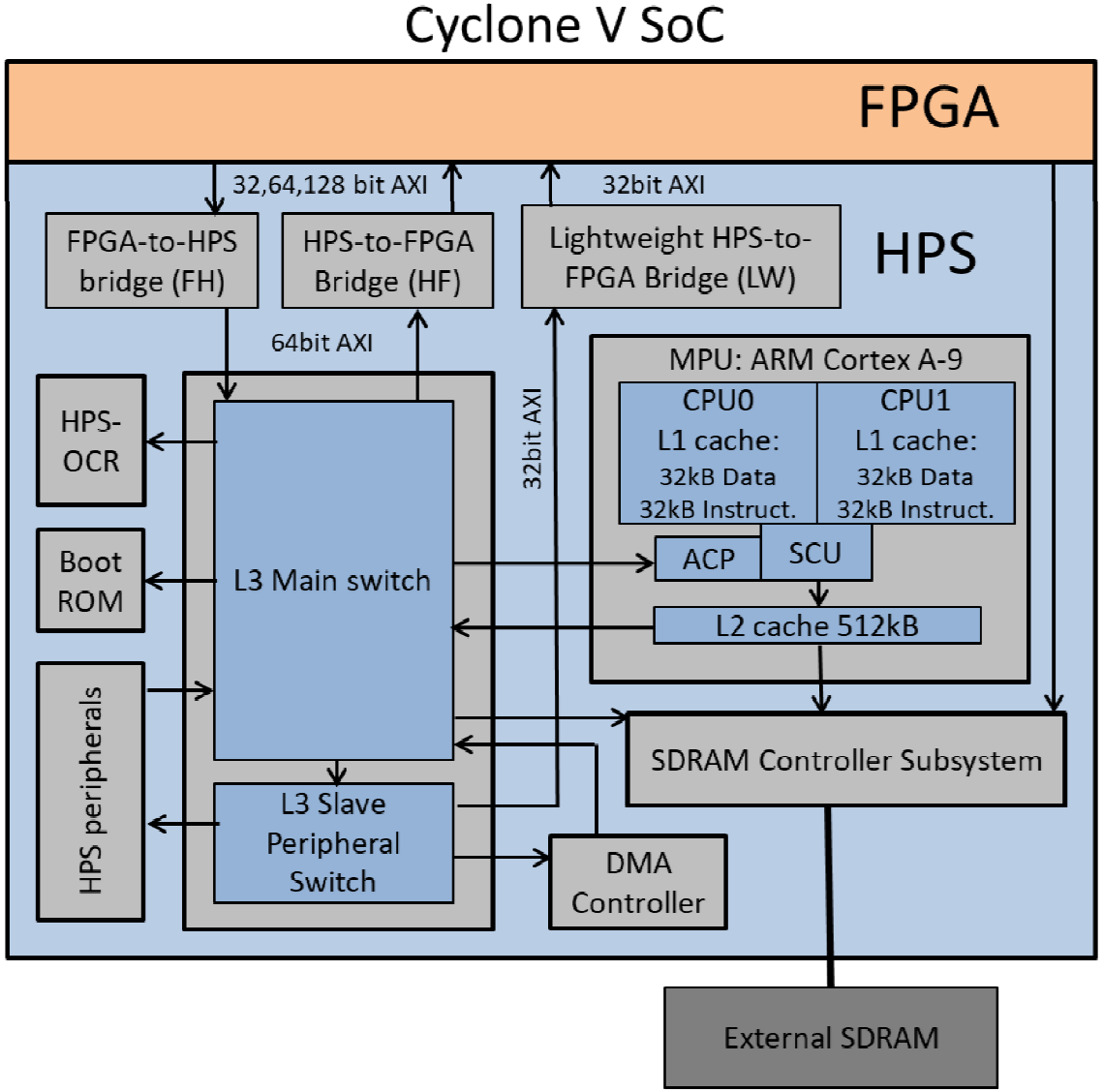
Therefore, it is possible to use the Cyclone V SoC in 3 different configurations:

- FPGA-only,
- HPS-only,
- HPS & FPGA.

Cyclone V SoC
Communication between HPS and FPGA

Generally communication between HPS and FPGA in Cyclone V SoC devices can be accomplished in the following ways:

1) **HPS-to-FPGA bridge**
   A high performance interface from HPS to FPGA. Transactions are usually conducted by the processor or Direct Memory Access (DMA) controllers present in HPS. Bridge is used for accessing FPGA logic, peripherals and memory.
2) **HPS-to-FPGA Lightweight bridge**
   A low performance interface to the FPGA fabric. Usually used by the processor to access control and status registers of the components implemented into FPGA.



Cyclone V SoC
Communication between HPS and FPGA

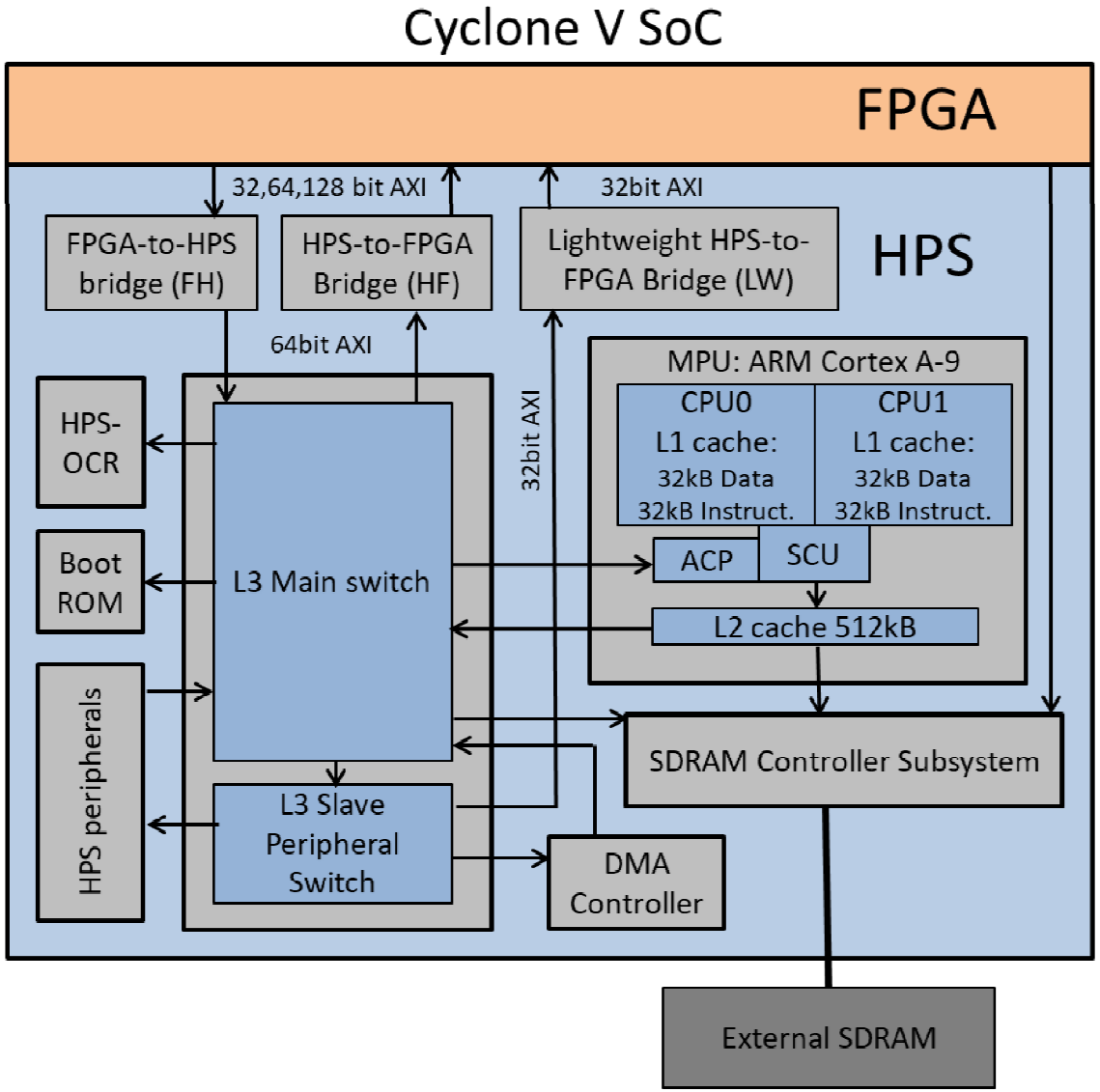
Generally communication between HPS and FPGA in Cyclone V SoC devices can be accomplished in the following ways:

3) FPGA-to-HPS bridge

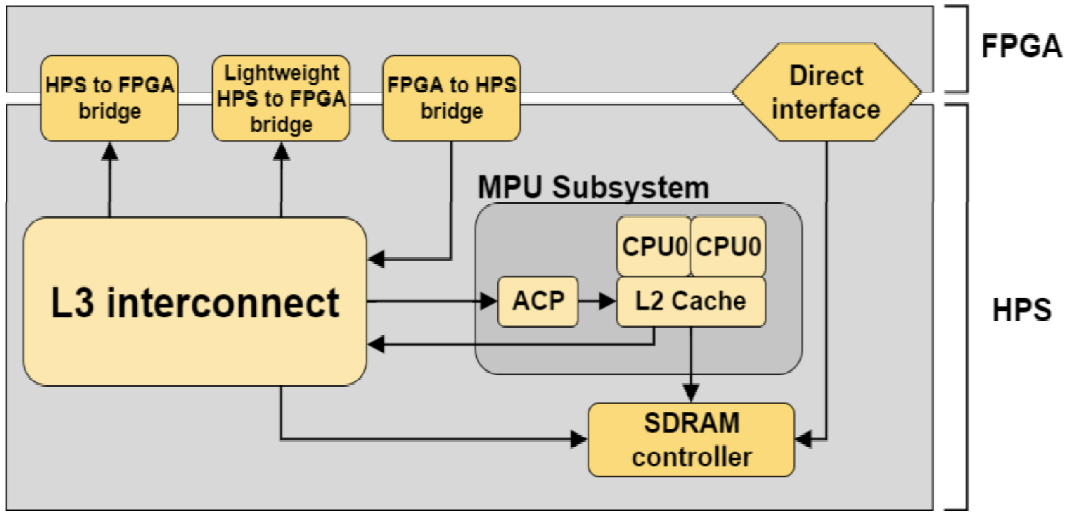
A high performance interface from FPGA to HPS peripherals and memory. Cached memory transactions are supported by adopting ARMs Accelerator Coherency Port (ACP).

4) FPGA-to-HPS SDRAM interface

A high performance interface from FPGA to HPS SDRAM controller. FPGA master has access to the processor's RAM. Data residing in processor's cache will result in errors, this issue must be addressed by the software.



Cyclone V SoC
FPGA to SDRAM data transfer

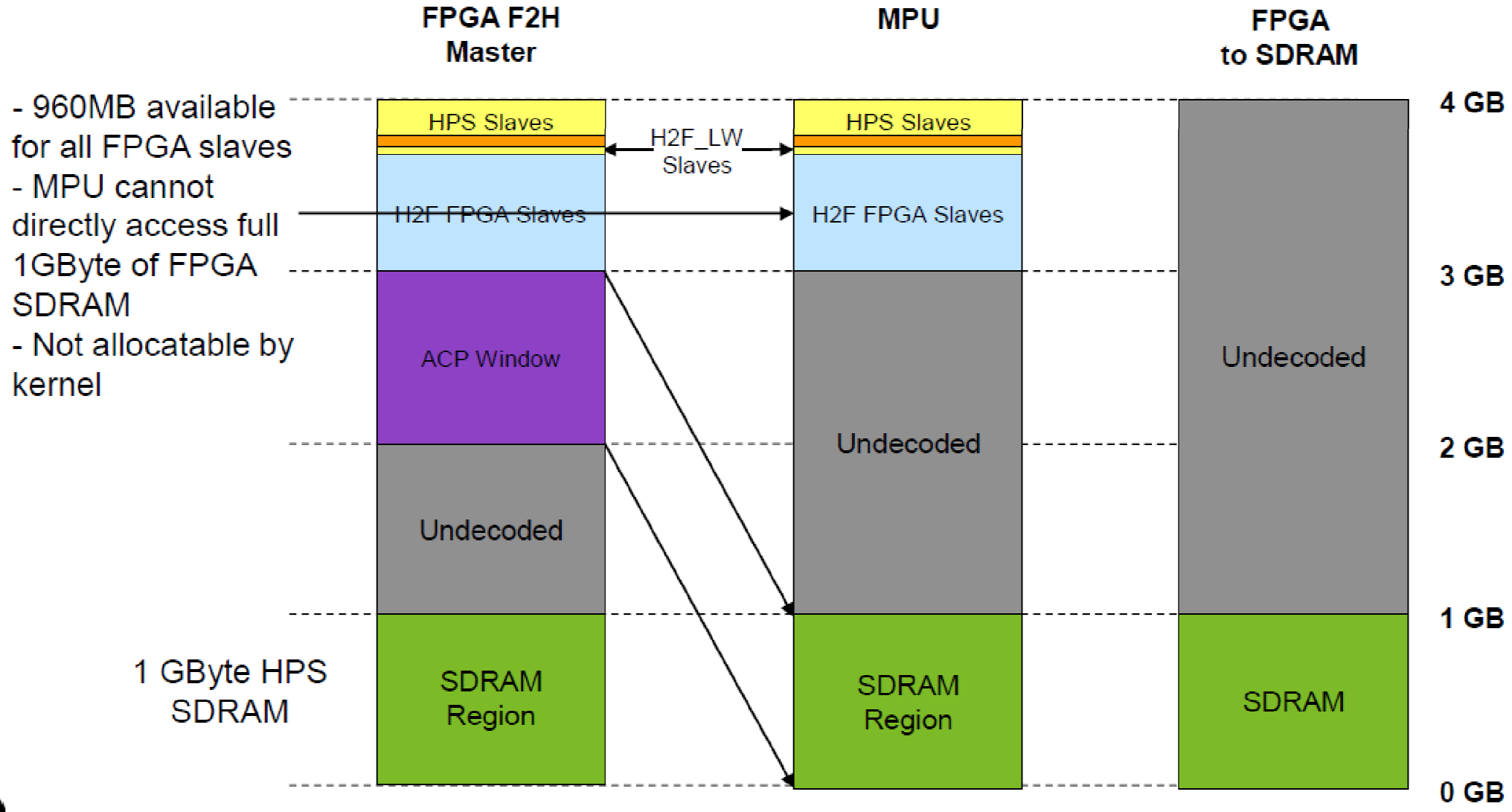


Data path	Bus width	Maximum throughput	Saturation frequency
FPGA-L3-SDRAM	32 bits	5.05 Gbps	120 MHz
	64 bits	10.10 Gbps	120 MHz
	128 bits	10.52 Gbps	65 MHz
FPGA-L3-ACP-SDRAM	32 bits	6.90 Gbps	-
	64 bits	8.64 Gbps	120 MHz
	128 bits	11.26 Gbps	90 MHz
FPGA-SDRAM	32 bits	7.52 Gbps	-
	64 bits	14.64 Gbps	-
	128 bits	17.68 Gbps	80 MHz
	256 bits	20.08 Gbps	45 MHz

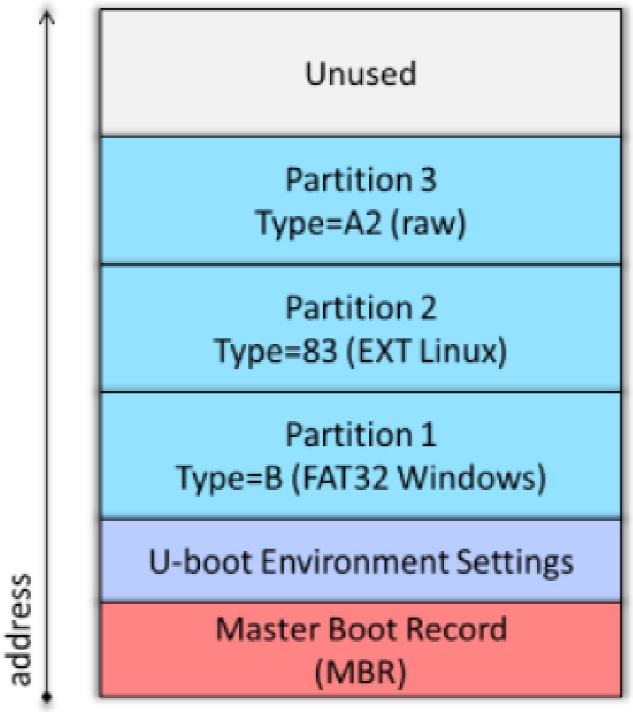
FPGA to SDRAM data transfer:

- **FPGA-SDRAM** – FPGA Master directly interacts with SDRAM controller.
- **FPGA-L3-SDRAM** – FPGA Master interacts with SDRAM controller via L3 interconnect.
- **FPGA-L3-ACP-SDRAM** – FPGA Master interacts with SDRAM controller via L3 interconnect and ACP.

Cyclone V SoC Memory Map



Cyclone V SoC
SD Card Image



Location	File Name	Desciption
Partition 1 (FAT32)	socfpga.dtb	Device Tree Blob
	soc_system.rbf	FPGA configuration file
	u-boot.scr	U-Boot script: configures FPGA and loads kernel
	zImage	Compressed Linux kernel image file
Partition 2 (EXT3)	Various	Linux root file system
Partition 3 (A2 raw)	n/a	Preloader image(s)
	n/a	U-Boot image

Cyclone V SoC
HSP Peripherals

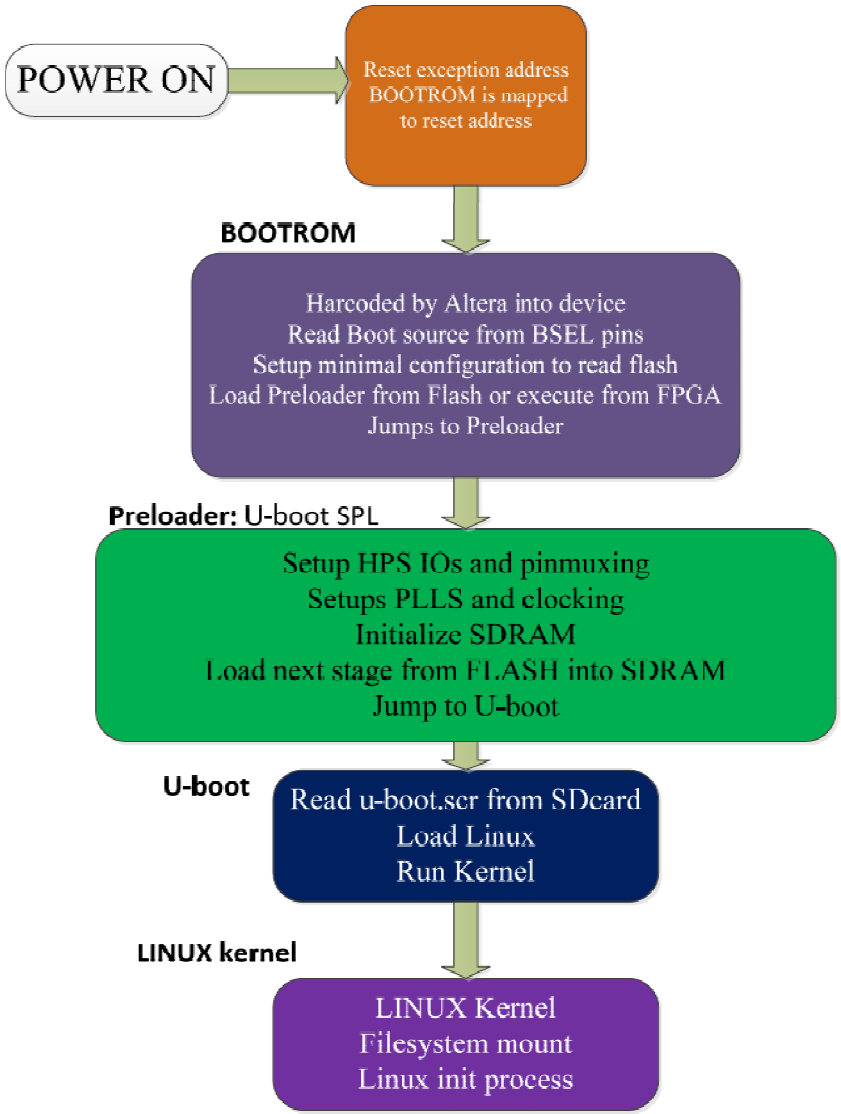
Possibilities of using HPS peripheral systems :

- HSP Peripherals (e.g.: UART, SPI) + dedicated HPS pins;
- HPS Peripherals + any FPGA pins;
- HPS pins as GPIO;
- FPGA pins controlled by HPS (LOANIO).

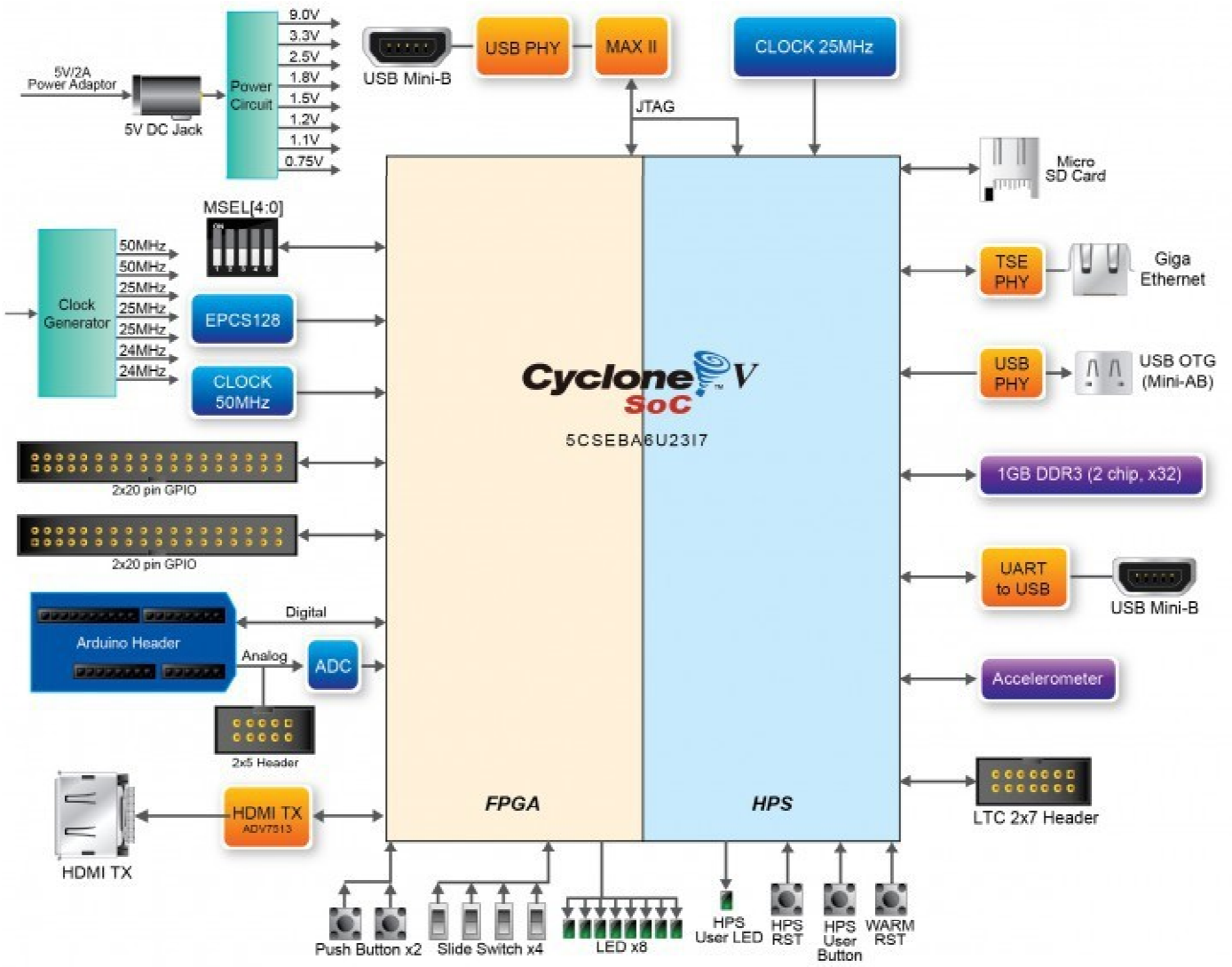
Cyclone V SoC
HSP Peripherals Mux Table

Peripherals Mux Table					
RGMII0_TX_CLK			EMAC0.TX_CLK (Set0)	GPIO00	LOANIO00
RGMII0_TXD0		USB1.D0 (Set0)	EMAC0.TXD0 (Set0)	GPIO01	LOANIO01
RGMII0_TXD1		USB1.D1 (Set0)	EMAC0.TXD1 (Set0)	GPIO02	LOANIO02
RGMII0_TXD2		USB1.D2 (Set0)	EMAC0.TXD2 (Set0)	GPIO03	LOANIO03
RGMII0_TXD3		USB1.D3 (Set0)	EMAC0.TXD3 (Set0)	GPIO04	LOANIO04
RGMII0_RXD0		USB1.D4 (Set0)	EMAC0.RXD0 (Set0)	GPIO05	LOANIO05
RGMII0_MDIO	I2C2.SDA (Set0)	USB1.D5 (Set0)	EMAC0.MDIO (Set0)	GPIO06	LOANIO06
RGMII0_MDC	I2C2.SCL (Set0)	USB1.D6 (Set0)	EMAC0.MDC (Set0)	GPIO07	LOANIO07
RGMII0_RX_CTL		USB1.D7 (Set0)	EMAC0.RX_CTL (Set0)	GPIO08	LOANIO08
RGMII0_TX_CTL			EMAC0.TX_CTL (Set0)	GPIO09	LOANIO09
RGMII0_RX_CLK		USB1.CLK (Set0)	EMAC0.RX_CLK (Set0)	GPIO10	LOANIO10
RGMII0_RXD1		USB1.STP (Set0)	EMAC0.RXD1 (Set0)	GPIO11	LOANIO11
RGMII0_RXD2		USB1.DIR (Set0)	EMAC0.RXD2 (Set0)	GPIO12	LOANIO12
RGMII0_RXD3		USB1.NXT (Set0)	EMAC0.RXD3 (Set0)	GPIO13	LOANIO13
NAND_ALE	QSPI.SS3 (Set1) (Set0)	EMAC1.TX_CLK (Set0)	NAND.ALE (Set0)	GPIO14	LOANIO14
NAND_CE	USB1.D0 (Set1)	EMAC1.TXD0 (Set0)	NAND.CE (Set0)	GPIO15	LOANIO15
NAND_CLE	USB1.D1 (Set1)	EMAC1.TXD1 (Set0)	NAND.CLE (Set0)	GPIO16	LOANIO16
NAND_RE	USB1.D2 (Set1)	EMAC1.TXD2 (Set0)	NAND.RE (Set0)	GPIO17	LOANIO17
NAND_RB	USB1.D3 (Set1)	EMAC1.TXD3 (Set0)	NAND.RB (Set0)	GPIO18	LOANIO18
NAND_DQ0		EMAC1.RXD0 (Set0)	NAND.DQ0 (Set0)	GPIO19	LOANIO19
NAND_DQ1	I2C3.SDA (Set0)	EMAC1.MDIO (Set0)	NAND.DQ1 (Set0)	GPIO20	LOANIO20
NAND_DQ2	I2C3.SCL (Set0)	EMAC1.MDC (Set0)	NAND.DQ2 (Set0)	GPIO21	LOANIO21
NAND_DQ3	USB1.D4 (Set1)	EMAC1.RX_CTL (Set0)	NAND.DQ3 (Set0)	GPIO22	LOANIO22
NAND_DQ4	USB1.D5 (Set1)	EMAC1.TX_CTL (Set0)	NAND.DQ4 (Set0)	GPIO23	LOANIO23
NAND_DQ5	USB1.D6 (Set1)	EMAC1.RX_CLK (Set0)	NAND.DQ5 (Set0)	GPIO24	LOANIO24
NAND_DQ6	USB1.D7 (Set1)	EMAC1.RXD1 (Set0)	NAND.DQ6 (Set0)	GPIO25	LOANIO25
NAND_DQ7		EMAC1.RXD2 (Set0)	NAND.DQ7 (Set0)	GPIO26	LOANIO26
NAND_WP	QSPI.SS2 (Set1) (Set0)	EMAC1.RXD3 (Set0)	NAND.WP (Set0)	GPIO27	LOANIO27
NAND_WE		QSPI.SS1 (Set0)	NAND.WE (Set0)	GPIO28	LOANIO28
QSPI_IO0	USB1.CLK (Set1)		QSPI.IO0 (Set1) (Set0)	GPIO29	LOANIO29
QSPI_IO1	USB1.STP (Set1)		QSPI.IO1 (Set1) (Set0)	GPIO30	LOANIO30
QSPI_IO2	USB1.DIR (Set1)		QSPI.IO2 (Set1) (Set0)	GPIO31	LOANIO31
QSPI_IO3	USB1.NXT (Set1)		QSPI.IO3 (Set1) (Set0)	GPIO32	LOANIO32
QSPI_SS0			QSPI.SS0 (Set1) (Set0)	GPIO33	LOANIO33
QSPI_CLK			QSPI.CLK (Set1) (Set0)	GPIO34	LOANIO34
QSPI_SS1			QSPI.SS1 (Set1)	GPIO35	LOANIO35

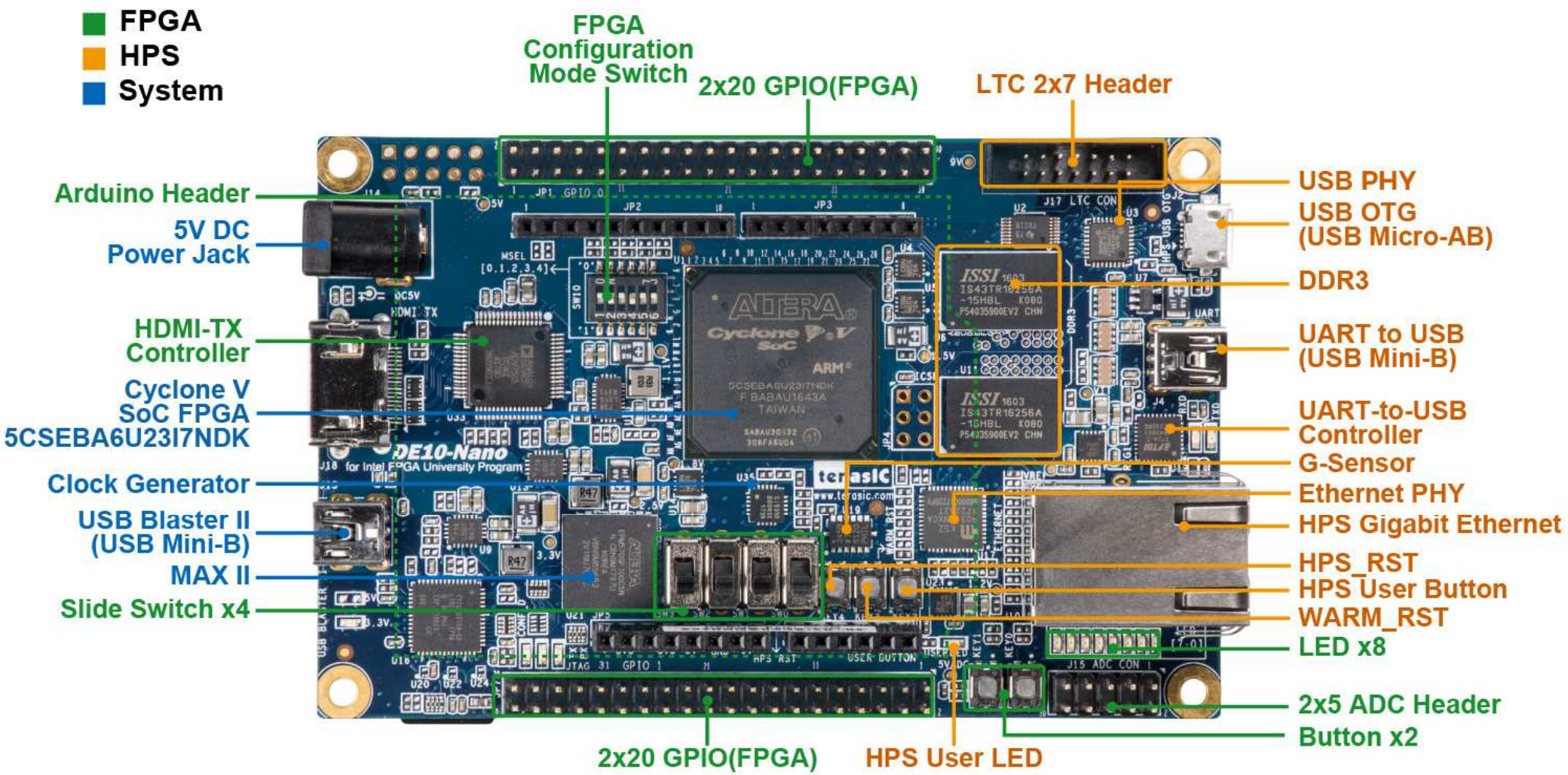
Cyclone V SoC
HPS Booting Process



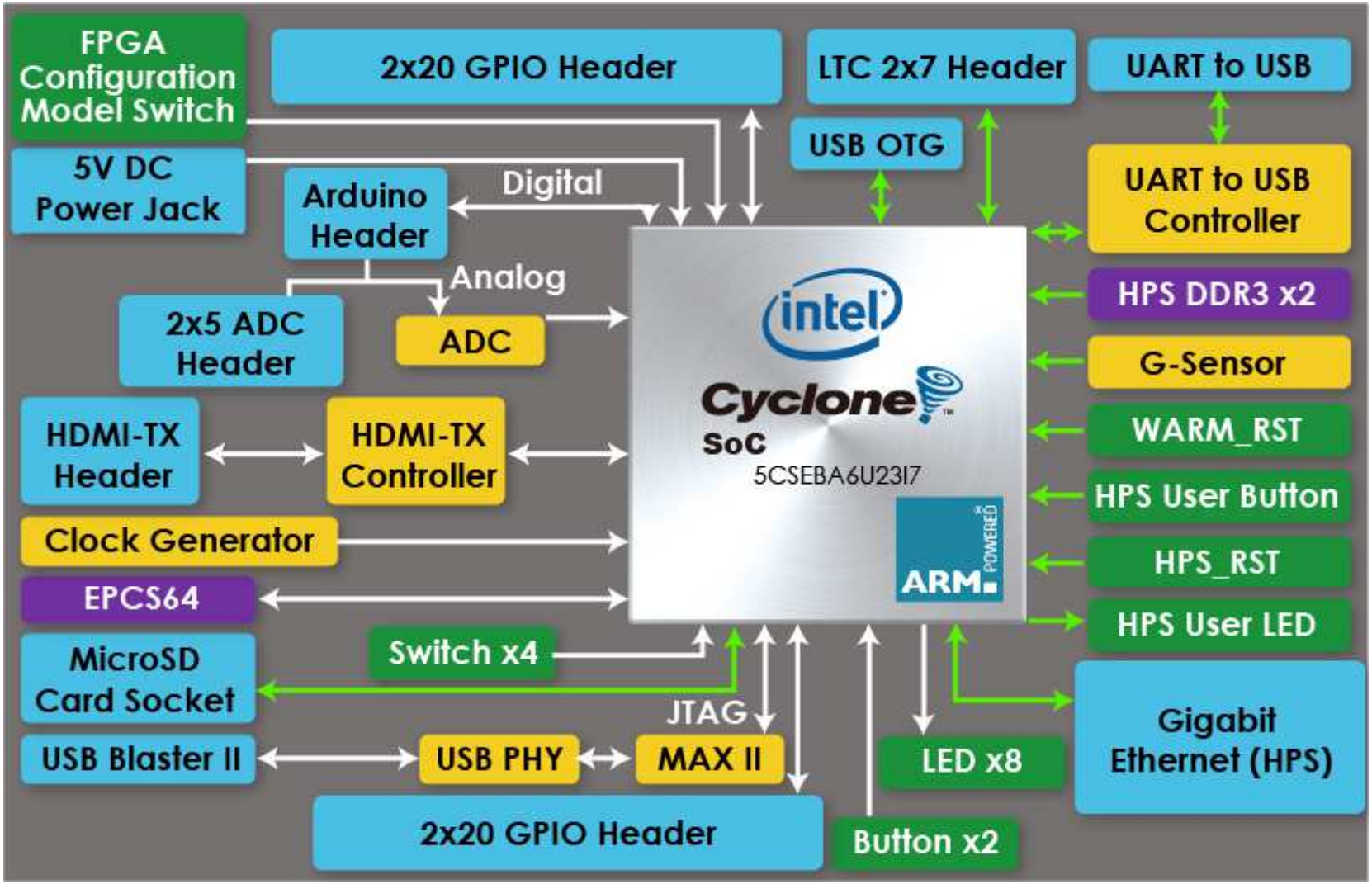
DE10 -Nano


5V/2A Power Adaptor
5V DC Jack
Power Circuit
9.0V
3.3V
2.5V
1.8V
1.5V
1.2V
1.1V
0.75V
USB Mini-B
USB PHY
MAX II
CLOCK 25MHz
JTAG
Micro SD Card
MSEL[4:0]
Clock Generator
50MHz
50MHz
25MHz
25MHz
25MHz
24MHz
24MHz
EPCS128
CLOCK 50MHz
TSE PHY
Giga Ethernet
USB PHY
USB OTG (Mini-AB)
Cyclone V SoC
5CSEBA6U23I7
2x20 pin GPIO
2x20 pin GPIO
1GB DDR3 (2 chip, x32)
UART to USB
USB Mini-B
Digital
Arduino Header
Analog
ADC
Accelerometer
2x5 Header
HDMI TX
ADV7513
HDMI TX
FPGA
HPS
LTC 2x7 Header
Push Button x2
Slide Switch x4
LED x8
HPS User LED
HPS RST
HPS User Button
WARM RST

DE10 -Nano


FPGA
HPS
System
FPGA Configuration Mode Switch
2x20 GPIO(FPGA)
LTC 2x7 Header
Arduino Header
5V DC Power Jack
HDMI-TX Controller
Cyclone V SoC FPGA 5CSEBA6U23I7NDK
Clock Generator
USB Blaster II (USB Mini-B)
MAX II
Slide Switch x4
USB PHY
USB OTG (USB Micro-AB)
DDR3
UART to USB (USB Mini-B)
UART-to-USB Controller
G-Sensor
Ethernet PHY
HPS Gigabit Ethernet
HPS_RST
HPS User Button
WARM_RST
LED x8
2x5 ADC Header
Button x2
2x20 GPIO(FPGA)
HPS User LED

DE10 - Nano


FPGA Configuration Model Switch
2x20 GPIO Header
LTC 2x7 Header
UART to USB
5V DC Power Jack
Arduino Header
Digital
USB OTG
UART to USB Controller
Analog
2x5 ADC Header
ADC
intel
Cyclone
SoC
5CSEBA6U23I7
HPS DDR3 x2
G-Sensor
HDMI-TX Header
HDMI-TX Controller
WARM_RST
HPS User Button
Clock Generator
HPS_RST
EPCS64
HPS User LED
MicroSD Card Socket
Switch x4
JTAG
Gigabit Ethernet (HPS)
USB Blaster II
USB PHY
MAX II
LED x8
2x20 GPIO Header
Button x2
ARM
POWERED

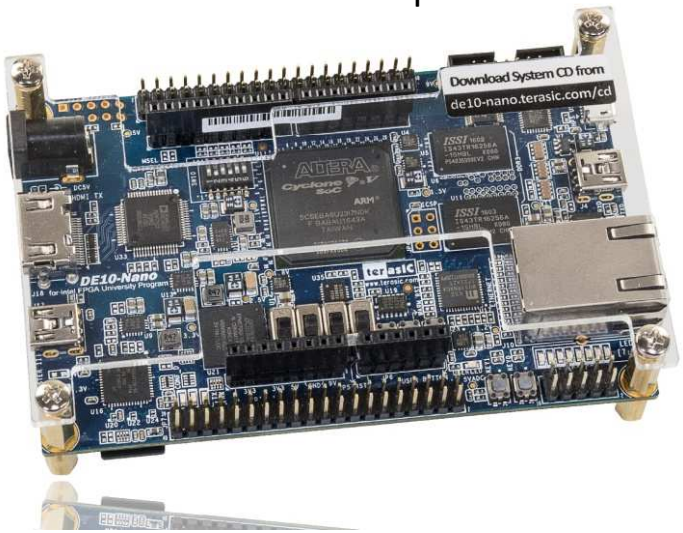
DE10 - Nano

FPGA Device

- Intel Cyclone® V SE 5CSEBA6U23I7 device (110K LEs)
- Serial configuration device – EPCS64 (revision B2 or later)
- USB-Blaster II onboard for programming; JTAG Mode
- HDMI TX, compatible with DVI 1.0 and HDCP v1.4
- 2 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50MHz clock sources from the clock generator
- Two 40-pin expansion headers
- One Arduino expansion header (Uno R3 compatibility), can be connected with Arduino shields
- One 10-pin Analog input expansion header (shared with Arduino Analog input)
- A/D converter, 4-pin SPI interface with FPGA

HPS (Hard Processor System)

- 800MHz Dual-core ARM Cortex-A9 processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- USB OTG Port, USB Micro-AB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header



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[1] dr hab. inż. Maciej Petko, prof. AGH - Wykład