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XSB Board V1.0 Manual

How to install and use
your new XSB Board

Table of Contents

1 Preliminaries

Getting Help!

Here are some places to get help if you encounter problems:

- If you can't get the XSB Board hardware to work, send an e-mail message describing your problem to help@xess.com or submit a problem report at http://www.xess.com/help.html. Our web site also has
  - answers to frequently-asked-questions,
  - example designs for the XS Boards,
  - application notes,
  - a place to sign-up for our email forum where you can post questions to other XS Board users.

Take Notice!!

- If you are connecting a 9VDC power supply to your XSB Board, please make sure the center terminal of the plug is positive and the outer sleeve is negative!
- **The SpartanIIE FPGA on the XSB Board is not 5V-tolerant!** Do not connect the expansion headers on the XSB Board to signals that exceed 3.3V.

Packing List

Here is what you should have received in your package:

- an XSB Board;
- a 6-foot, 25-wire cable with a male DB25 connector at each end;
- an XSTOOLs CDROM with software utilities and documentation for using the XSB Board.

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XSB Overview

The XSB Board brings you the power of the XILINX SpartanIIE FPGA embedded in a framework for processing video and audio signals. The XSB Board has a single SpartanIIE FPGA containing 300K system gates. The XSB can digitize PAL, SECAM, or NTSC video with up to 9-bits of resolution on the red, green, and blue channels and can output video images through an 80 MHz, 30-bit video DAC. The XSB can also process stereo audio signals with up to 20 bits of resolution and a bandwidth of 50 KHz. A 256K x 16 SRAM and an 8M x 16 SDRAM are provided for local buffering of signals and data. You can also connect an IDE hard disk or Compact Flash card for even more storage.

The XSB Board has a variety of interfaces for communicating with the outside world: parallel and serial ports, USB 2.0 port, and 10/100 Ethernet MAC+PHY interface. There are also two independent expansion ports that connect directly to the SpartanIIE FPGA and another that connects through the Ethernet controller.

You can configure the XSB Board through a PC parallel port or from a bitstream stored in a 4 Mbit Flash RAM. The Flash RAM can also store data for use by the FPGA after configuration is complete.

XSB Board Features

The XSB Board includes the following resources:

- Programmable logic chips:

  XILINX SpartanIIE FPGA: The SpartanIIE FPGA is the main repository of programmable logic on the XSB Board.

  XILINX XC9572XL CPLD: The CPLD is used to manage the configuration of the FPGA via the parallel port or Flash RAM.

- PLL-based programmable oscillator that provides clock signals for the FPGA, CPLD, video decoder and Ethernet controller derived form a 24 MHz base frequency.

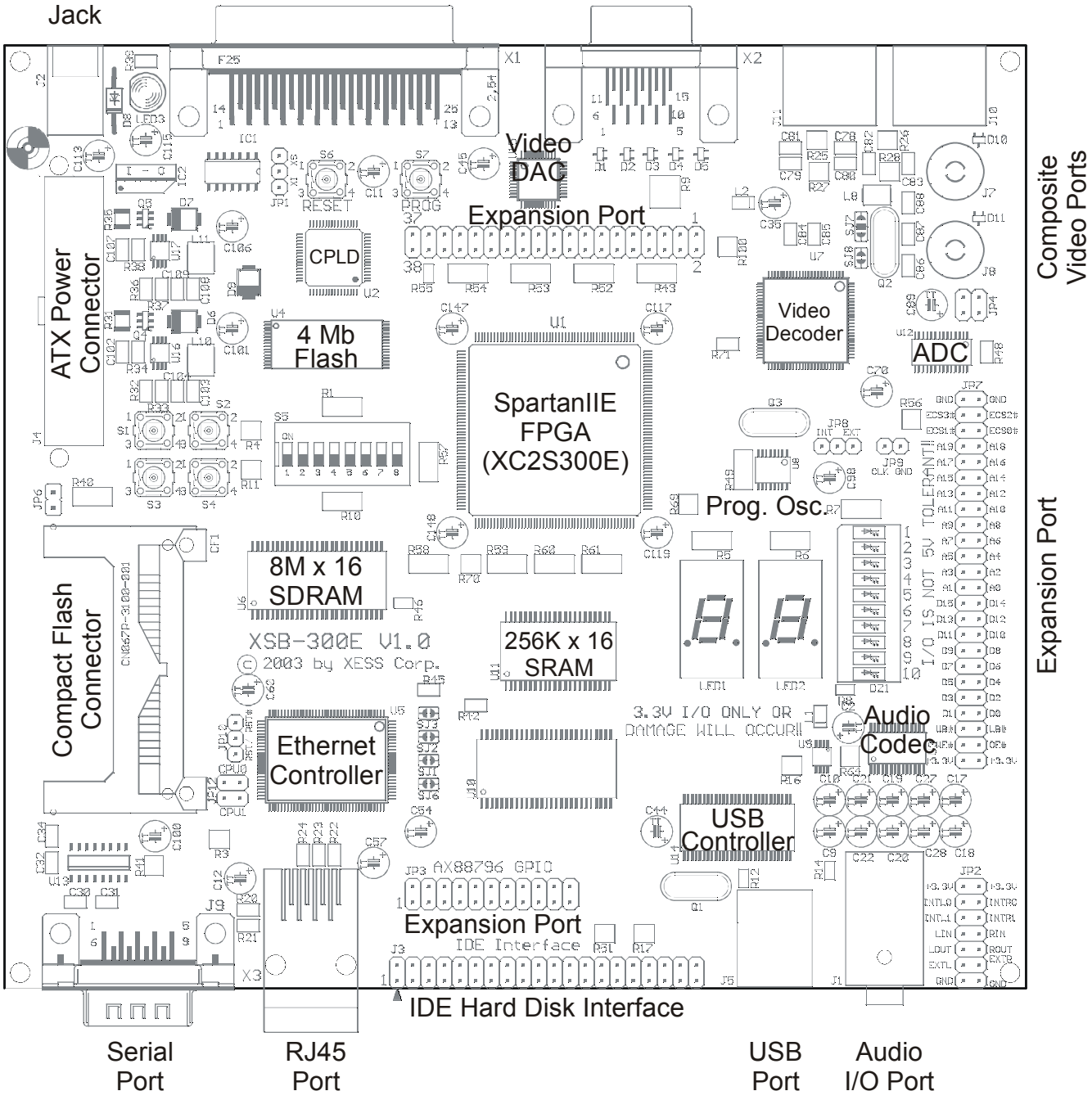
- 4 Mbit Flash RAM that can store multiple configurations or general-purpose data for the FPGA.

- 256K x 16 SRAM and 16M x 16 SDRAM for general-purpose data storage.

- Video decoder that accepts up to six NTSC/PAL/SECAM signals through dual RCA jacks and dual S-video connectors and outputs the digitized signal to the FPGA.

- Video DAC with three 10-bit DACs that are used by the FPGA to output red, green and blue signals to a VGA monitor.
- Stereo codec that lets the FPGA digitize as many as four stereo audio channels at up to 50 KHz with 20 bits of resolution and generate a single stereo output.
- ADC allows sampling of signals with 12-bits of resolution at 30 MSPS.
- IDE hard disk ATA interface for massive, non-volatile storage.
- Compact Flash interface supports True IDE, PC Card Memory and PC Card I/O modes.
- 10/100 Ethernet MAC+PHY that allows the FPGA to access a LAN at up to 100 Mbps.
- Single USB 2.0 port provides the FPGA with up to 480 Mbps of serial I/O.
- Single RS232 serial port connects directly to the FPGA.
- One 34-pin and one 44-pin expansion header that each interface the FPGA to external circuitry through 0.1" headers. There is an additional 18-pin expansion header that can be accessed through the Ethernet controller.
- Four pushbuttons and one eight-position DIP switch provide general-purpose inputs to the FPGA and CPLD.
- Two LED digits and one LED bargraph let the FPGA and CPLD display status information.
- ATX power connector or 9V DC power jack lets the XSB Board receive power from a standard ATX power supply or a 9V DC power supply.

The locations of these resources are indicated in the simplified view of the XSB Board shown below. Each of these resources will be described in the following section.


9V DC Jack
Parallel Port
VGA Port
S-Video Ports
Composite Video Ports
Expansion Port
Video DAC
Expansion Port
ATX Power Connector
CPLD
4 Mb Flash
SpartanIIE FPGA (XC2S300E)
Video Decoder
ADC
Prog. Osc.
8M x 16 SDRAM
256K x 16 SRAM
Compact Flash Connector
XSB-300E V1.0
© 2003 by XESS Corp.
Ethernet Controller
Audio Codec
USB Controller
AX88796 GPIO
Expansion Port
IDE Interface
IDE Hard Disk Interface
Serial Port
RJ45 Port
USB Port
Audio I/O Port

3
Installation

Installing the XSTOOLs Software

Run the SETUP.EXE file on the XSTOOLs CDROM. This will install the utilities and configuration files for testing and programming your XSB Board.

Unpacking the Board

You should place the XSB Board on a non-conducting surface.

Configuring the Jumpers

Your XSB Board should arrive with the shunts set on the jumpers in their default arrangement. The minimal shunt arrangement to allow testing of your XSB Board is as follows:

1. Place a shunt in the “XS” position on jumper JP1.

2. Place a shunt in the “INT” position of jumper JP8.

Applying Power

You can supply the XSB Board with power in two ways:

1. ***Recommended!*** Attach an ATX PC power supply to connector J4.

2. Attach a 9V DC power supply with a 2.1mm, center-positive plug to jack J2. The power supply must be able to source at least 1.0 A.

LED3 will glow when the power is on.

Connecting to a PC

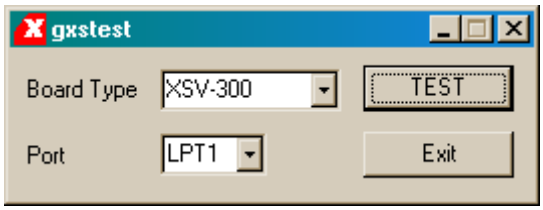
One DB25 connector on the 6-foot cable should be attached to connector X1 on the XSB Board and the other end should plug into the parallel port connector of a PC.

Testing Your XSB Board

Once your XSB Board is installed and the jumpers are in their default configuration, you can test the board using the GUI-based GXSTEST utility as follows.

You start GXSTEST by clicking on the 

icon placed on the desktop during the XSTOOLS installation. This brings up the window shown below.



Next you select the parallel port that your XSB Board is connected to from the Port pulldown list. GXSTEST starts with parallel port LPT1 as the default, but you can also select LPT2 or LPT3 depending upon the configuration of your PC.

After selecting the parallel port, select either XSB-300E item in the Board Type pulldown list. Then click on the TEST button to start the testing procedure. GXSTEST will configure the FPGA to perform a test procedure on your XSB Board. After several seconds you will see a **O** displayed on the LED digit if the test completes successfully. Otherwise an **E** will be displayed if the test fails. A status window will also appear on your PC screen informing you of the success or failure of the test.

If your XSB Board fails the test, you will be shown a checklist of common causes for failure. If none of these causes applies to your situation, then test the XSB Board using another PC. In our experience, 99.9% of all problems are due to the parallel port. If you cannot get your board to pass the test even after taking these steps, then contact XESS Corp for further assistance.

As a result of testing the XSB Board, the CPLD is programmed with a parallel port interface found in the dwnldpar.svf bitstream file located within the XSTOOLS\XSB folder. This CPLD configuration provides the general-purpose parallel port interface that is used in all applications of the XSB Board.

Setting the XSB Board Clock Oscillator Frequency

The XSB Board has a PLL-based programmable oscillator (a Cypress CY22393FC). An external 24 MHz crystal frequency is scaled up internally to generate frequencies of 100 MHz, 368.4 MHz and 399 MHz. These frequencies are then divided internally to provide the following clocks to the XSB Board circuitry:

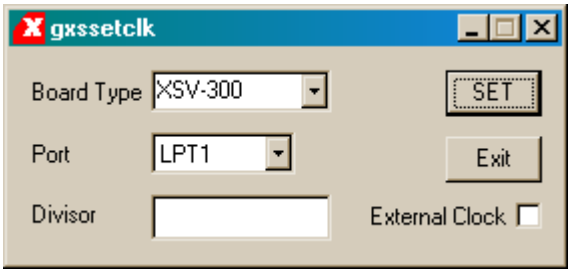
CY22393 Output	Frequency (MHz)	XSB Clock	Function
CLKA	24.576	VIDIN-CLK	Video input clock
CLKB	66.5	SDRAM-CLK	SDRAM clock
CLKC	100	FPGA-CLK0	General-purpose FPGA clock
CLKD	50	FPGA-CLK1	General-purpose FPGA clock
CLKE	25	ETHER-CLK	Ethernet clock
XBUF	24	CPLD-CLK	CPLD clock

FPGA-CLK1 is derived from a 100 MHz master frequency that is divided by factors of 1, 2, ... up to 127 to get clock frequencies of 100 MHz, 50 MHz, ... down to 787 KHz, respectively. The divided frequency is sent to the FPGA as a clock signal.

You can change the divisor for FPGA-CLK1 with the GUI-based GXSSETCLK as follows.

You start GXSSETCLK by clicking on the 

icon placed on the desktop during the XSTOOLS installation. This brings up the window shown below.



Your next step is to select the parallel port that your XSB Board is connected to from the Port pulldown list. Then select the XSB-300E Board from the Board Type pulldown list.

Next you enter a divisor between 1 and 127 into the Divisor text box and then click on the SET button. The new divisor will be programmed into the oscillator chip. **Note that the divisor will be lost if power to the board is interrupted and FPGA-CLK1 will go back to its default frequency!**

Checking the External Clock checkbox has no effect on the XSB-300E Board. If you wish to use an external clock source, you must place the shunt on jumper J8 at the "EXT" position and then input your clock signal through the JP9 connector. The external clock will then replace FPGA-CLK0 that goes to the FPGA..

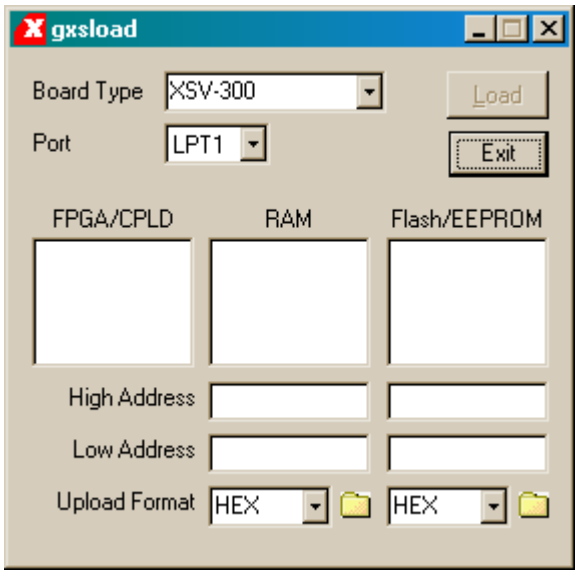
Note that GXSSETCLK reprograms the FPGA on the XSB Board in order to access the programmable oscillator. You will need to reprogram the FPGA with the bitstream for your particular application circuit after you have set the clock divisor.

Programming the Interface

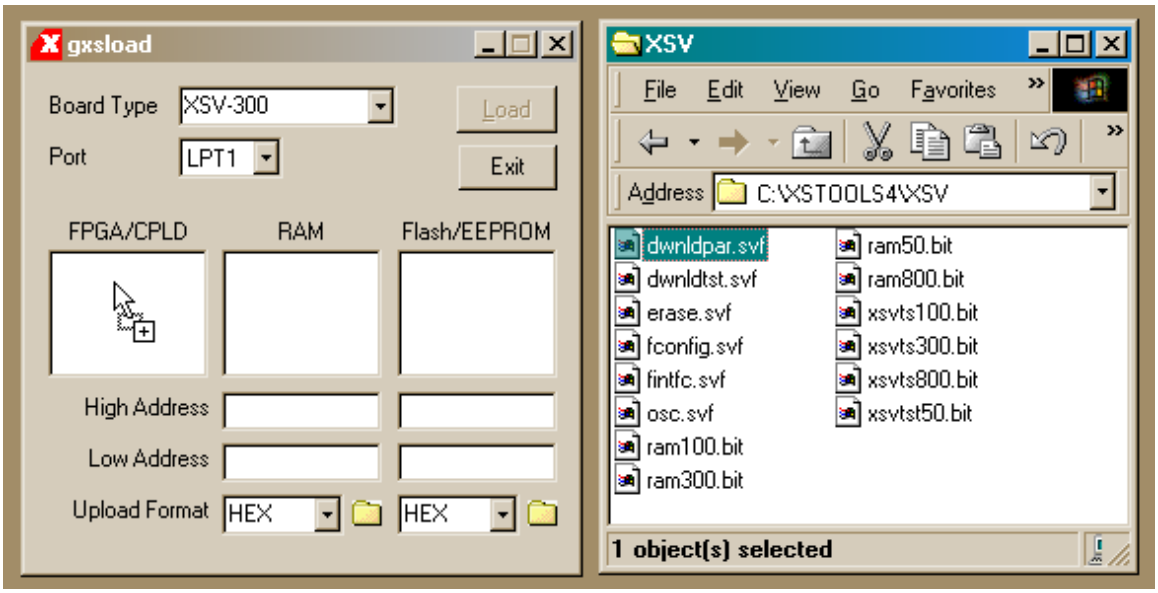
The FPGA is the main repository of programmable logic on the XSB Board. The CPLD manages the configuration of the FPGA via the parallel port or from the Flash memory. Therefore, the CPLD must be configured so that it implements the necessary interface. The CPLD stores its configuration in its internal non-volatile memory so the interface is restored each time power is applied to the XSB Board (unless the interface circuit is erased).

The CPLD is configured with an interface by using the GXSLOAD software utility. You start GXSLOAD by clicking on the 

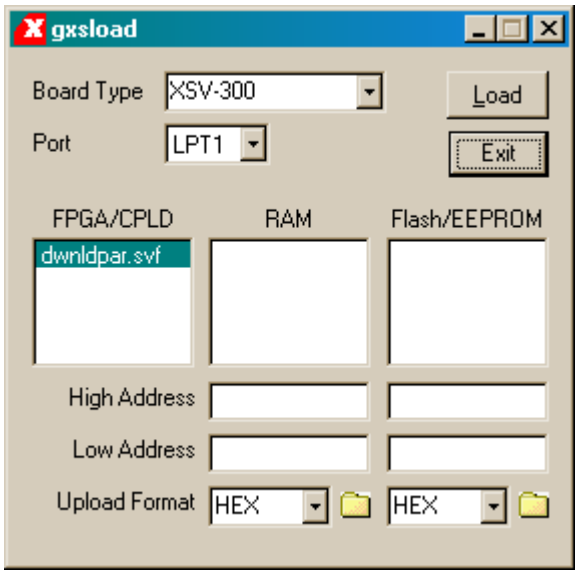
icon placed on the desktop during the XSTOOLS installation. This brings up the window shown below. Select type of board you are using and the parallel port to which it is connected as described previously.



After setting the board type and parallel port, you can download an .SVF file to the CPLD on your XSB Board simply by dragging it into the FPGA/CPLD area of the GXSLOAD window as shown below. For example, to program the CPLD with the standard parallel port interface, drag the dwnldpar.svf file from the XSTOOLS\XSB folder.



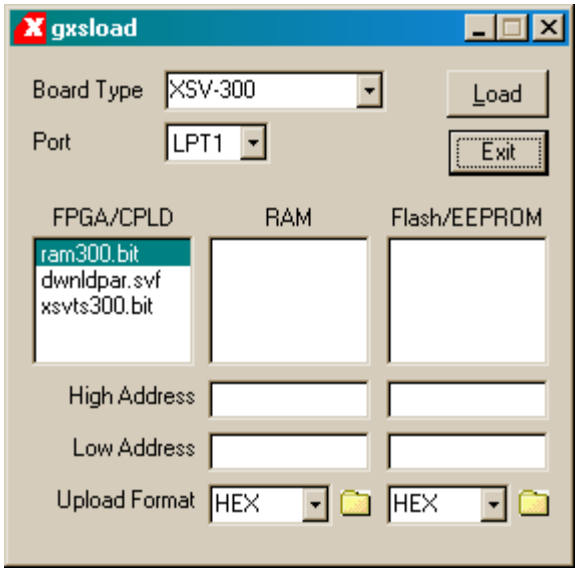
Once you release the left mouse button and drop the file, the highlighted file name appears in the FPGA/CPLD area and the Load button in the GXSLOAD window is enabled. Clicking on the Load button will begin sending the .SVF file to the CPLD on the XSB Board through the parallel port connection. During the downloading process, GXSLOAD will display the name of the file and the progress of the current download.



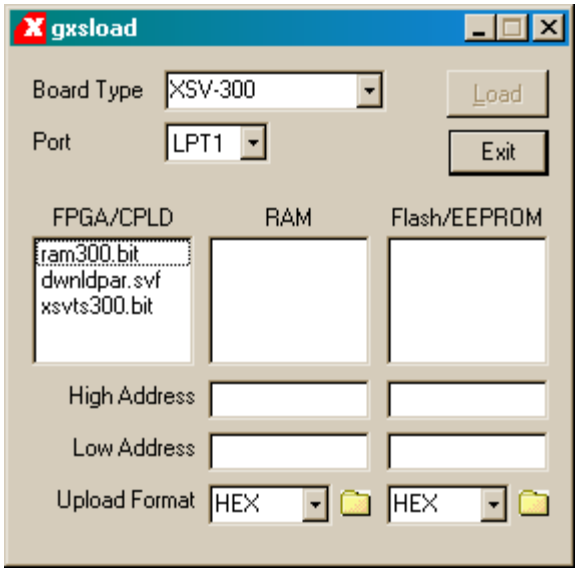
Downloading FPGA Configuration Bitstreams

Once the CPLD is programmed with the downloading interface circuit, you can download bitstreams into the FPGA using the GXSLOAD utility. Drag & drop one or more .BIT files for the type of SpartanIIE FPGA on your XSB Board into the FPGA/CPLD area of the GXSLOAD window. Clicking your mouse on a file name will highlight the name and select

the file for downloading. Only one bitstream file at a time can be selected. Clicking on the Load button causes the highlighted configuration bitstream to pass through the parallel port and CPLD and then into the FPGA.



Double-clicking the highlighted file will deselect it so no file will be downloaded. Doing this disables the Load button.



Storing Non-Volatile Designs in Your XSB Board

The FPGA on the XSB Board stores its configuration in an on-chip SRAM which is erased whenever power is removed. Once your design is finalized, you may want to store the bitstream in the Flash device on the XSB Board which configures the FPGA for operation as soon as power is applied.

Before downloading to the Flash, the bitstream file must be converted into a .EXO or .MCS format using one of the following commands:

```
promgen –u 0 file.bit –p exo –s 512

promgen –u 0 file.bit –p mcs –s 512
```

In the commands shown above, the bitstream in the file.bit file is transformed into an .EXO or .MCS file format starting at address zero and proceeding upward until an upper limit of 512 KBytes is reached.

After the .EXO or .MCS file is generated, it is loaded into the Flash device by dragging it into the Flash/EEPROM area and clicking on the Load button. This activates the following sequence of steps:

1. The entire Flash device is erased.

2. The CPLD on the XSB Board is reprogrammed to create an interface between the Flash device and the PC parallel port. (This interface is stored in the fintfc.svf bitstream file located within the XSTOOLS\XSB folder.)

3. The contents of the .EXO or .MCS file are downloaded into the Flash through the parallel port.

4. The CPLD is reprogrammed to create a circuit that configures the FPGA with the contents of the Flash when power is applied to the XSB Board. (This configuration loader is stored in the fconfig.svf bitstream file located within the XSTOOLS\XSB folder.)

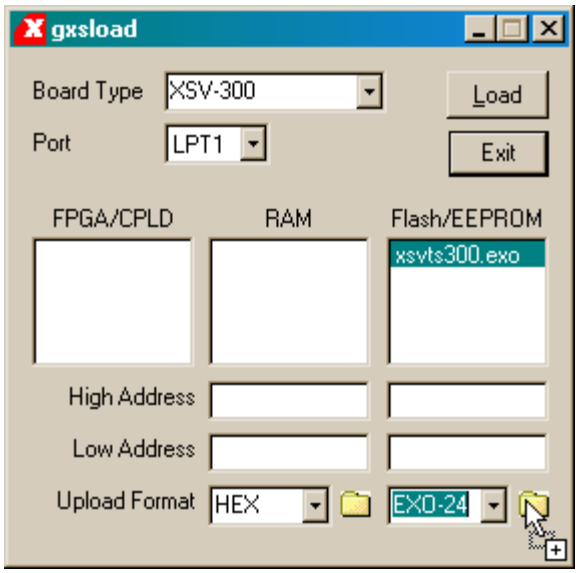
Multiple files can be stored in the Flash device just by dragging them into the Flash/EEPROM area, highlighting the files to be downloaded and clicking the Load button. (Note that anything previously stored in the Flash will be erased.) This is useful if you need to store information in the Flash in addition to the FPGA bitstream. Files are selected and de-selected for downloading just by clicking on their names in the Flash/EEPROM area. **The address ranges of the data in each file should not overlap or this will corrupt the data stored in the Flash device!**

You can also examine the contents of the Flash device by uploading it to the PC. To upload data from an address range in the Flash, type the upper and lower bounds of the range into the High Address and Low Address fields below the Flash/EEPROM area, and select the format in which you would like to store the data using the Upload Format pulldown list. Then click on the file icon and drag & drop it into any folder. This activates the following sequence of steps:

1. The CPLD and FPGA on the XSB Board are reprogrammed to create an interface between the Flash device and the PC parallel port.

2. The Flash data between the high and low addresses (inclusive) is uploaded through the parallel port.

3. The uploaded data is stored in a file named FLSHUPLD with an extension that reflects the file format.



The uploaded data can be stored in the following formats:

MCS: Intel hexadecimal file format. This is the same format generated by the promgen utility with the –p mcs option.

HEX: Identical to MCS format.

EXO-16: Motorola S-record format with 16-bit addresses (suitable for 64 KByte uploads only).

EXO-24: Motorola S-record format with 24-bit addresses. This is the same format generated by the promgen utility with the –p exo option.

EXO-32: Motorola S-record format with 32-bit addresses.

XESS-16: XESS hexadecimal format with 16-bit addresses. (This is a simplified file format that does not use checksums.)

XESS-24: XESS hexadecimal format with 24-bit addresses.

XESS-32: XESS hexadecimal format with 32-bit addresses.

After the data is uploaded from the Flash, the CPLD is left with the standard parallel port interface programmed into it. You will need to reprogram the CPLD with the Flash configuration circuit if you want it to configure itself from the Flash. (This configuration circuit is stored in the fconfig.svf bitstream file located within the XSTOOLS\XSB folder.)

Downloading and Uploading Data to the RAM in Your XSB Board

The XSB Board contains a 256K x 16 SRAM and an 8M x 16 SDRAM whose contents can be downloaded and uploaded by GXSLOAD. This is useful for initializing the SRAM/SDRAM with data for use by the FPGA and then reading the SRAM/SDRAM contents after the FPGA has operated upon it. The SRAM/SDRAM is loaded with data by dragging & dropping one or more .EXO, .MCS, .HEX, and/or .XES files into the RAM area of the GXSLOAD window and then clicking on the Load button. This activates the following sequence of steps:

1. The FPGA on the XSB Board is reprogrammed to create an interface between the SRAM/SDRAM devices and the PC parallel port. (This interface is stored in the ramintfc.bit bitstream file located within the XSTOOLS\XSB folder. **The CPLD must have previously been loaded with the dwnldpar.svf file found in the same folder.**)

2. The contents of the .EXO, .MCS, .HEX or .XES files are downloaded into the SRAM/SDRAM through the parallel port. **The data in the files will overwrite each other if their address ranges overlap.**

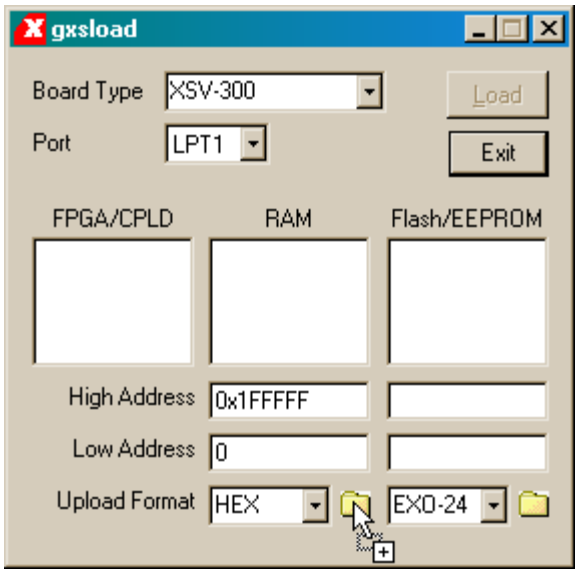
3. If any file is highlighted in the FPGA/CPLD area, then this bitstream is loaded into the FPGA or CPLD on the XSB Board. Otherwise the FPGA remains configured with the interface to the SRAM/SDRAM.

You can also examine the contents of the SRAM/SDRAM device by uploading it to the PC. To upload data from an address range in the SRAM/SDRAM, type the upper and lower bounds of the range into the High Address and Low Address fields below the RAM area, and select the format in which you would like to store the data using the Upload Format pulldown list. Then click on the file icon and drag & drop it into any folder. This activates the following sequence of steps:

1. The FPGA is reprogrammed to create an interface between the RAM device and the PC parallel port.

2. The SRAM/SDRAM data between the high and low addresses (inclusive) is uploaded through the parallel port.

3. The uploaded data is stored in a file named RAMUPLD with an extension that reflects the file format.



The 16-bit data words in the SRAM/SDRAM are mapped into the eight-bit data format of the .HEX, .MCS, .EXO and .XES files using a Big Endian style. That is, the 16-bit word at address *N* in the SRAM/SDRAM is stored in the eight-bit file with the upper eight bits at location *2N* and the lower eight bits at location *2N+1*. This byte-ordering applies for both SRAM/SDRAM uploads and downloads.

With respect to the GXSLOAD upload/download process, the SDRAM is located in the byte address range [0x0000000–0x0FFFFFF] and the SRAM is between byte addresses [0x1000000–0x107FFFF].

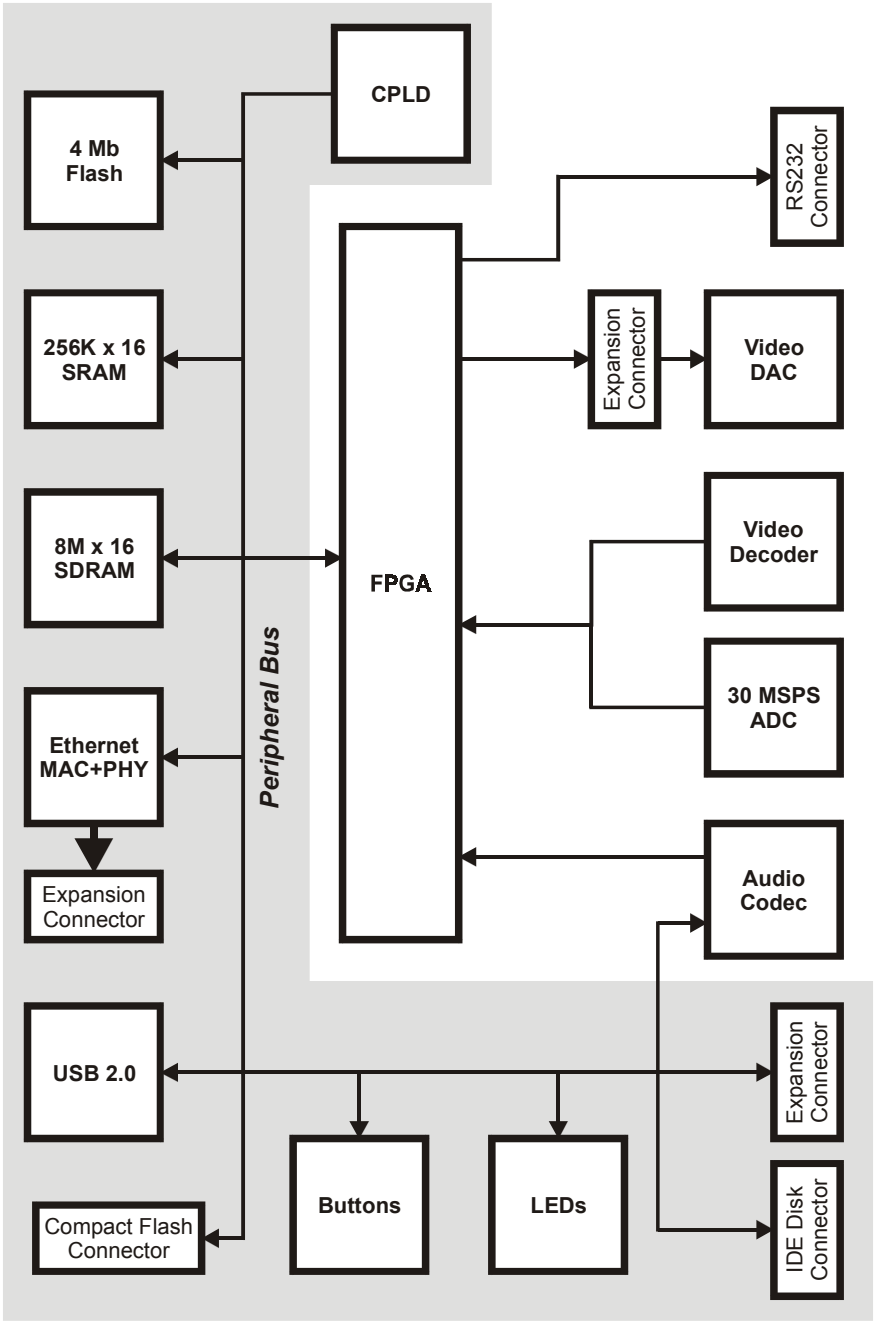
4

XSB Circuitry

This section describes the various sections of the XSB Board and shows how the I/O of the FPGA and CPLD are connected to the rest of the circuitry. The schematics which follow are less detailed so as to simplify the descriptions. Please refer to the complete schematics at the end of this document if you need more details.

Overview of the XSB Board Circuitry

The XSB Board has two major groups of components that connect to the FPGA: 1) those with dedicated buses, and 2) those that share a peripheral bus. Components that process video and audio data streams use dedicated buses, while all other components use the shared Peripheral Bus. (The audio codec actually connects to both types of buses: it is loaded with configuration data through the Peripheral Bus but it sends and receives digitized audio data through a dedicated bus.) The chip-selects for components on the Peripheral Bus are controlled by the FPGA to prevent contention.



Programmable Logic: SpartanIIE FPGA and XC9500 CPLD

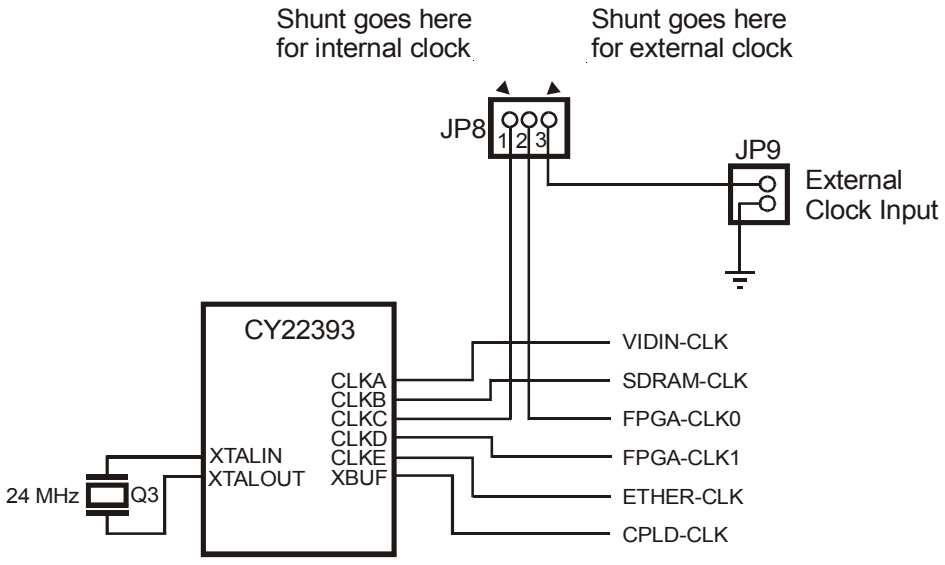
The XSB Board contains two programmable logic chips:

- A XILINX SpartanIIE 300-Kgate FPGA in a 208-pin QFP package (XC2S300E-6PQ208C) is the main repository of programmable logic on the XSB Board.
- A XILINX XC9500 CPLD (XC9572XL-10VQ64C) manages the configuration of the FPGA via the parallel port or Flash RAM.

Programmable Oscillator

A PLL-based programmable oscillator (CY22393FC) generates the clocks for the various sections of the XSB Board. An external 24 MHz crystal frequency is scaled up internally to generate frequencies of 100 MHz, 368.4 MHz and 399 MHz. These frequencies are then divided internally to provide the following clocks to the XSB Board circuitry:

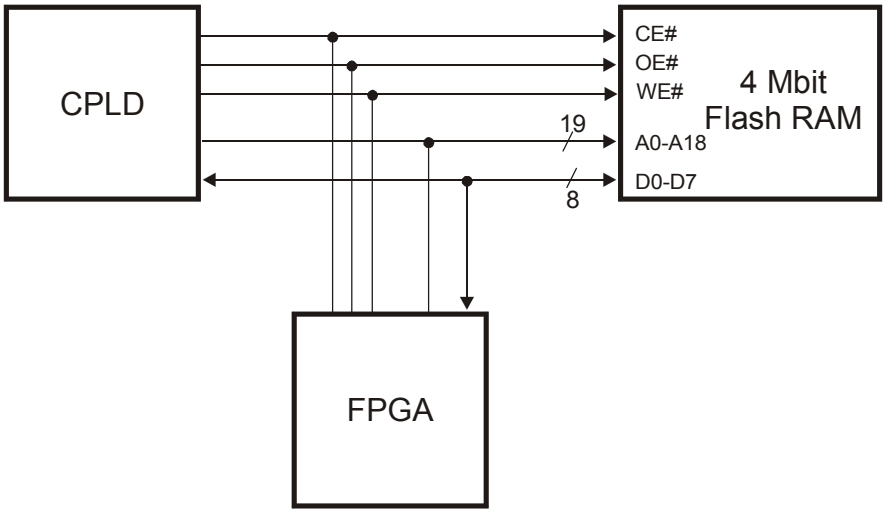
CY22393 Output	Frequency (MHz)	XSB Clock	Function	Connects to...
CLKA	24.576	VIDIN-CLK	Video decoder input clock	SAA7114 pin 7
CLKB	66.5	SDRAM-CLK	SDRAM clock	FPGA pin 80, SDRAM pin 38
CLKC	100	FPGA-CLK0	General-purpose FPGA clock	FPGA pin 182
CLKD	50	FPGA-CLK1	General-purpose FPGA clock	FPGA pin 77
CLKE	25	ETHER-CLK	Ethernet clock	AX88796 pin 79
XBUF	24	CPLD-CLK	CPLD clock	CPLD pin 17



To sync the XSB circuitry with an external system, you can insert an external clock signal through jumper JP9 and place a shunt at position “EXT” of jumper JP8. This external clock replaces the FPGA-CLK0 output from the oscillator.

4 Mbit Flash RAM

A Flash RAM (AT49LV040-12TC) with 4 Mbits of storage (512K × 8) is connected to both the FPGA and CPLD. Typically, the CPLD will program the Flash with data passed through the parallel port. If the data is an FPGA configuration bitstream then the CPLD can be configured to program the FPGA with the Flash bitstream whenever the XSB Board is powered up. After power-up, the FPGA can read and/or write the Flash. (Of course, the CPLD and FPGA have to be programmed such that they do not conflict if both are trying to access the Flash.) The Flash can be disabled by raising the FLASH-CE# pin to Vcc.



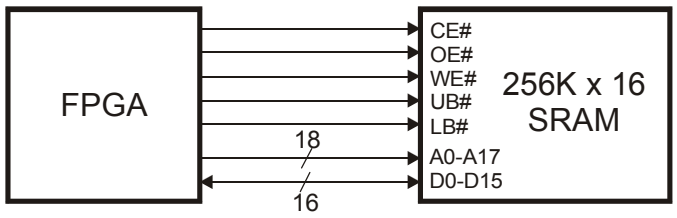
The connections between the Flash RAM, FPGA and CPLD are listed below.

Peripheral Bus	Flash Pin	FPGA Pin	CPLD Pin	Function
FLASH-CE#	CE#	57	11	Flash chip-enable (active low)
PB-OE#	OE#	125	12	Flash output-enable (active-low)
PB-WE#	WE#	123	49	Flash write-enable (active-low)
PB-A0	A0	83	1	Flash address line 0
PB-A1	A1	84	64	Flash address line 1
PB-A2	A2	86	63	Flash address line 2
PB-A3	A3	87	62	Flash address line 3
PB-A4	A4	88	61	Flash address line 4
PB-A5	A5	89	60	Flash address line 5
PB-A6	A6	93	59	Flash address line 6
PB-A7	A7	94	58	Flash address line 7
PB-A8	A8	100	45	Flash address line 8
PB-A9	A9	101	44	Flash address line 9
PB-A10	A10	102	57	Flash address line 10
PB-A11	A11	109	43	Flash address line 11
PB-A12	A12	110	56	Flash address line 12
PB-A13	A13	111	46	Flash address line 13

Peripheral Bus	Flash Pin	FPGA Pin	CPLD Pin	Function
PB-A14	A14	112	47	Flash address line 14
PB-A15	A15	113	52	Flash address line 15
PB-A16	A16	114	51	Flash address line 16
PB-A17	A17	115	48	Flash address line 17
PB-A18	A18	121	42	Flash address line 18
PB-D0	D0	153	2	Flash data line 0
PB-D1	D1	145	4	Flash data line 1
PB-D2	D2	141	5	Flash data line 2
PB-D3	D3	135	6	Flash data line 3
PB-D4	D4	126	7	Flash data line 4
PB-D5	D5	120	8	Flash data line 5
PB-D6	D6	116	9	Flash data line 6
PB-D7	D7	108	10	Flash data line 7

SRAM

The FPGA has access to a 256K x 16 SRAM (TC55V16256FT-15) for local storage of data.



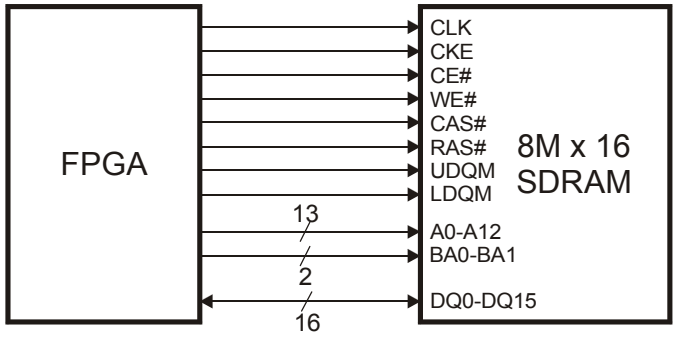
The FPGA pins connect to the SRAM as shown below:

Peripheral Bus	SRAM Pin	FPGA Pin	Function
RAM-CE#	CE#	147	SRAM chip-enable (active low)
PB-OE#	OE#	125	SRAM output-enable (active-low)
PB-WE#	WE#	123	SRAM write-enable (active-low)
PB-UB#	UB#	146	Enable upper-byte of databus (active-low)
PB-LB#	LB#	140	Enable lower byte of databus (active-low)
PB-A0	A0	83	SRAM address line 0
PB-A1	A1	84	SRAM address line 1
PB-A2	A2	86	SRAM address line 2
PB-A3	A3	87	SRAM address line 3
PB-A4	A4	88	SRAM address line 4
PB-A5	A5	89	SRAM address line 5

Peripheral Bus	SRAM Pin	FPGA Pin	Function
PB-A6	A6	93	SRAM address line 6
PB-A7	A7	94	SRAM address line 7
PB-A8	A8	100	SRAM address line 8
PB-A9	A9	101	SRAM address line 9
PB-A10	A10	102	SRAM address line 10
PB-A11	A11	109	SRAM address line 11
PB-A12	A12	110	SRAM address line 12
PB-A13	A13	111	SRAM address line 13
PB-A14	A14	112	SRAM address line 14
PB-A15	A15	113	SRAM address line 15
PB-A16	A16	114	SRAM address line 16
PB-A17	A17	115	SRAM address line 17
PB-D0	D0	153	SRAM data line 0
PB-D1	D1	145	SRAM data line 1
PB-D2	D2	141	SRAM data line 2
PB-D3	D3	135	SRAM data line 3
PB-D4	D4	126	SRAM data line 4
PB-D5	D5	120	SRAM data line 5
PB-D6	D6	116	SRAM data line 6
PB-D7	D7	108	SRAM data line 7
PB-D8	D8	127	SRAM data line 8
PB-D9	D9	129	SRAM data line 9
PB-D10	D10	132	SRAM data line 10
PB-D11	D11	133	SRAM data line 11
PB-D12	D12	134	SRAM data line 12
PB-D13	D13	136	SRAM data line 13
PB-D14	D14	138	SRAM data line 14
PB-D15	D15	139	SRAM data line 15

SDRAM

The FPGA has access to an 8M x 16 SDRAM from Hynix (HY57V281620HCT-H) or Samsung (K4S281632E-TC75000) for storing larger amounts of data.



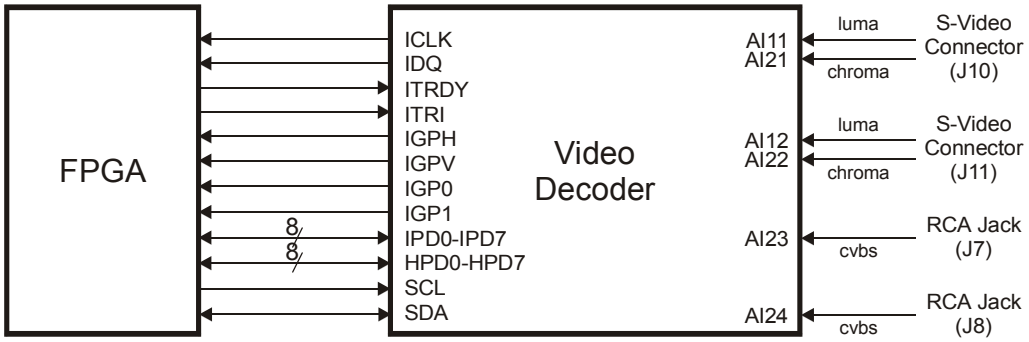
The FPGA pins connect to the SDRAM as shown below:

Peripheral Bus	SDRAM Pin	FPGA Pin	Function
SDRAM-CLK	CLK	80	SDRAM clock
SDRAM-CKE	CKE	99	SDRAM clock-enable (active-high)
SDRAM-CE#	CE#	98	SDRAM chip-enable (active low)
SDRAM-WE#	WE#	95	SDRAM write-enable (active-low)
SDRAM-CAS#	CAS#	96	SDRAM column address strobe
SDRAM-RAS#	RAS#	97	SDRAM row address strobe
PB-UB#	UDQM	146	Enable upper-byte of databus (active-low)
PB-LB#	LDQM	140	Enable lower byte of databus (active-low)
PB-A0	A0	83	SDRAM address line 0
PB-A1	A1	84	SDRAM address line 1
PB-A2	A2	86	SDRAM address line 2
PB-A3	A3	87	SDRAM address line 3
PB-A4	A4	88	SDRAM address line 4
PB-A5	A5	89	SDRAM address line 5

Peripheral Bus	SDRAM Pin	FPGA Pin	Function
PB-A6	A6	93	SDRAM address line 6
PB-A7	A7	94	SDRAM address line 7
PB-A8	A8	100	SDRAM address line 8
PB-A9	A9	101	SDRAM address line 9
PB-A10	A10	102	SDRAM address line 10
PB-A11	A11	109	SDRAM address line 11
PB-A12	A12	110	SDRAM address line 12
PB-A13	BA0	111	SDRAM bank address line 0
PB-A14	BA1	112	SDRAM bank address line 1
PB-D0	DQ0	153	SDRAM data line 0
PB-D1	DQ1	145	SDRAM data line 1
PB-D2	DQ2	141	SDRAM data line 2
PB-D3	DQ3	135	SDRAM data line 3
PB-D4	DQ4	126	SDRAM data line 4
PB-D5	DQ5	120	SDRAM data line 5
PB-D6	DQ6	116	SDRAM data line 6
PB-D7	DQ7	108	SDRAM data line 7
PB-D8	DQ8	127	SDRAM data line 8
PB-D9	DQ9	129	SDRAM data line 9
PB-D10	DQ10	132	SDRAM data line 10
PB-D11	DQ11	133	SDRAM data line 11
PB-D12	DQ12	134	SDRAM data line 12
PB-D13	DQ13	136	SDRAM data line 13
PB-D14	DQ14	138	SDRAM data line 14
PB-D15	DQ15	139	SDRAM data line 15

Video Decoder

The XSB Board can digitize NTSC, SECAM, and PAL video signals using a video decoder chip (SAA7114). The digitized video arrives at the FPGA over the IPD and HPD buses when IDQ is active. The arrival of video data is synchronized with the ICLK driven from the FPGA. The FPGA programs the video decoder options using the I^2C bus (SCL and SDA).



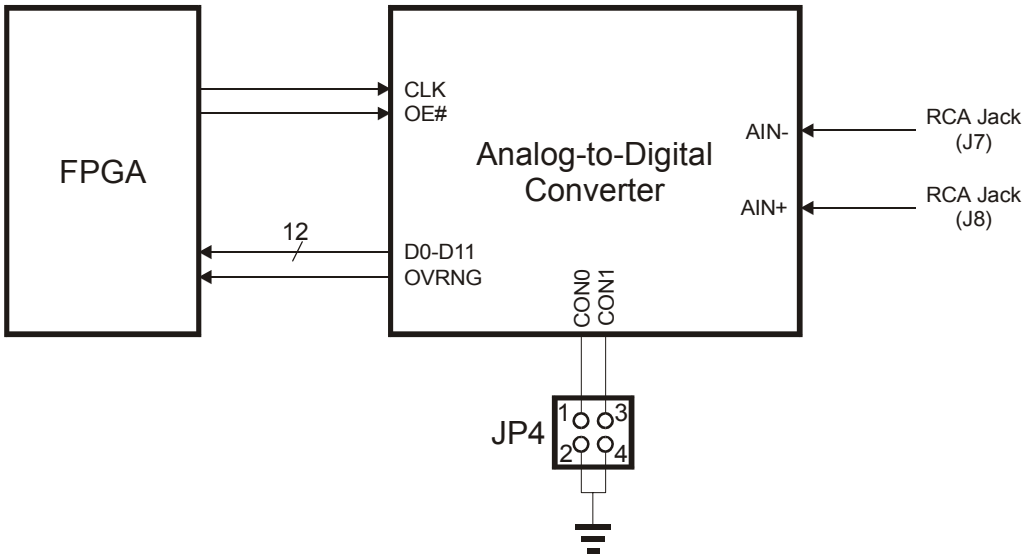
The FPGA pins connect to the video decoder as shown below:

Video Input Bus	I2C Bus	Vid. Dcdr. Pin	FPGA Pin	Function
VIDIN-ICLK		ICLK	185	Image interface clock output (to FPGA)
VIDIN-IDQ		IDQ	205	Image data qualifier output
VIDIN-ITRDY		ITRDY	206	Target ready input
VIDIN-ITRI		ITRI	204	Image port tristate input
VIDIN-IGPH		IGPH	200	Multi-purpose horizontal reference output
VIDIN-IGPV		IGPV	201	Multi-purpose vertical reference output
VIDIN-IGP0		IGP0	203	General-purpose output
VIDIN-IGP1		IGP1	202	General-purpose output
VIDIN-IPD0		IPD0	188	Image port data line 0
VIDIN-IPD1		IPD1	189	Image port data line 1
VIDIN-IPD2		IPD2	191	Image port data line 2
VIDIN-IPD3		IPD3	192	Image port data line 3
VIDIN-IPD4		IPD4	193	Image port data line 4
VIDIN-IPD5		IPD5	194	Image port data line 5

Video Input Bus	I2C Bus	Vid. Dcdr. Pin	FPGA Pin	Function
VIDIN-IPD6		IPD6	198	Image port data line 6
VIDIN-IPD7		IPD7	199	Image port data line 7
VIDIN-HPD0		HPD0	174	Image port data line 8
VIDIN-HPD1		HPD1	175	Image port data line 9
VIDIN-HPD2		HPD2	176	Image port data line 10
VIDIN-HPD3		HPD3	178	Image port data line 11
VIDIN-HPD4		HPD4	179	Image port data line 12
VIDIN-HPD5		HPD5	180	Image port data line 13
VIDIN-HPD6		HPD6	181	Image port data line 14
VIDIN-HPD7		HPD7	187	Image port data line 15
	I2C-SCL	SCL	6	I^2C clock
	I2C-SDA	SDA	5	I^2C data

Analog-to-Digital Converter

The XSB Board can digitize a differential analog signal using a 12-bit, 30 MSPS analog-to-digital converter (THS1230). The arrival of digitized data is synchronized with the CLK driven by the FPGA. The digitized signal comes from the ADC to the FPGA over the same pins used for the IPD and HPD buses of the video decoder interface. The OE# signal is used to prevent the ADC from interfering with the video decoder.



The ADC supports several operating modes determined by the arrangement of the shunts on jumper JP4:

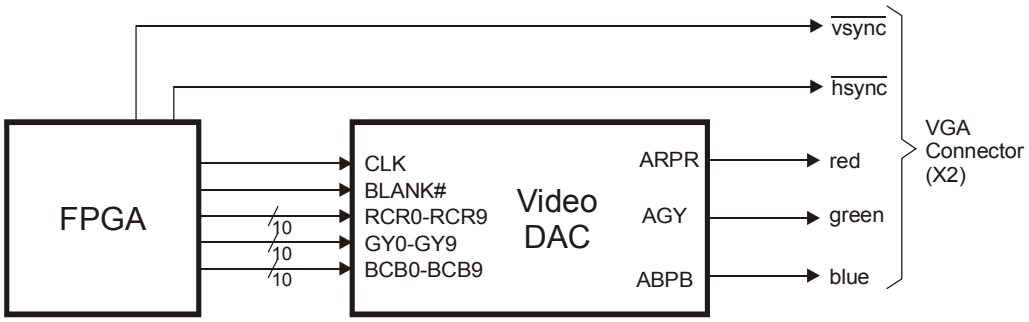
ADC Mode	JP4 Shunt Settings	
	CON1	CON0
Single-ended mode with offset	OFF	OFF
Differential mode x 0.5	OFF	ON
Single-ended mode / differential mode	ON	OFF
Device powered down	ON	ON

The FPGA pins connect to the ADC as shown below:

ADC Bus	Video Input Bus	ADC Pin	FPGA Pin	Function
ADC-CLK		CLK	3	ADC clock input
ADC-OE#		OE#	4	ADC output-enable (active-low)
	VIDIN-IPD0	D0	188	Digitized data output 0
	VIDIN-IPD1	D1	189	Digitized data output 1
	VIDIN-IPD2	D2	191	Digitized data output 2
	VIDIN-IPD3	D3	192	Digitized data output 3
	VIDIN-IPD4	D4	193	Digitized data output 4
	VIDIN-IPD5	D5	194	Digitized data output 5
	VIDIN-IPD6	D6	198	Digitized data output 6
	VIDIN-IPD7	D7	199	Digitized data output 7
	VIDIN-HPD0	D8	174	Digitized data output 8
	VIDIN-HPD1	D9	175	Digitized data output 9
	VIDIN-HPD2	D10	176	Digitized data output 10
	VIDIN-HPD3	D11	178	Digitized data output 11
	VIDIN-HPD4	OVRNG	179	Data out-of-range output

Video DAC

The FPGA uses a Texas Instruments video DAC (THS8133B) to generate the video signals for a VGA display. The FPGA passes 30-bit pixel data (10 bits for the red, green and blue color components) to the video DAC on each clock edge. The DAC generates the analog red, green and blue signals for the VGA display while the FPGA generates the horizontal and vertical sync pulses directly. The FPGA lowers the BLANK# signal when the pixels fall outside the desired visible area of the display.



The pin assignments for the connection of the FPGA to the VGA circuitry are shown below.

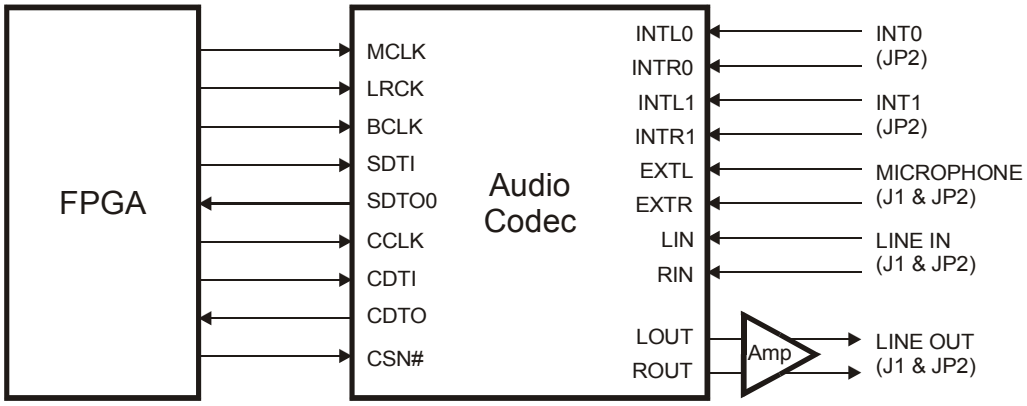
Video Output Bus	Video DAC Pin	FPGA Pin	Function
VIDOUT-CLK	CLK	23	Pixel clock input
VIDOUT-BLANK#	BLANK#	24	Video blanking signal (active-low)
VIDOUT-HSYNC#	NC	8	VGA horizontal sync pulse (active-low)
VIDOUT-VSYNC#	NC	7	VGA vertical sync pulse (active-low)
VIDOUT-RCR0	RCR0	41	Pixel red component bit 0
VIDOUT-RCR1	RCR1	40	Pixel red component bit 1
VIDOUT-RCR2	RCR2	36	Pixel red component bit 2
VIDOUT-RCR3	RCR3	35	Pixel red component bit 3
VIDOUT-RCR4	RCR4	34	Pixel red component bit 4
VIDOUT-RCR5	RCR5	33	Pixel red component bit 5
VIDOUT-RCR6	RCR6	31	Pixel red component bit 6
VIDOUT-RCR7	RCR7	30	Pixel red component bit 7
VIDOUT-RCR8	RCR8	29	Pixel red component bit 8
VIDOUT-RCR9	RCR9	27	Pixel red component bit 9

Video Output Bus	Video DAC Pin	FPGA Pin	Function
VIDOUT-GY0	GY0	9	Pixel green component bit 0
VIDOUT-GY1	GY1	10	Pixel green component bit 1
VIDOUT-GY2	GY2	11	Pixel green component bit 2
VIDOUT-GY3	GY3	15	Pixel green component bit 3
VIDOUT-GY4	GY4	16	Pixel green component bit 4
VIDOUT-GY5	GY5	17	Pixel green component bit 5
VIDOUT-GY6	GY6	18	Pixel green component bit 6
VIDOUT-GY7	GY7	20	Pixel green component bit 7
VIDOUT-GY8	GY8	21	Pixel green component bit 8
VIDOUT-GY9	GY9	22	Pixel green component bit 9
VIDOUT-BCB0	BCB0	42	Pixel blue component bit 0
VIDOUT-BCB1	BCB1	43	Pixel blue component bit 1
VIDOUT-BCB2	BCB2	44	Pixel blue component bit 2
VIDOUT-BCB3	BCB3	45	Pixel blue component bit 3
VIDOUT-BCB4	BCB4	46	Pixel blue component bit 4
VIDOUT-BCB5	BCB5	47	Pixel blue component bit 5
VIDOUT-BCB6	BCB6	48	Pixel blue component bit 6
VIDOUT-BCB7	BCB7	49	Pixel blue component bit 7
VIDOUT-BCB8	BCB8	55	Pixel blue component bit 8
VIDOUT-BCB9	BCB9	56	Pixel blue component bit 9

Stereo Codec

The XSB Board has a stereo codec (AK4565) that accepts two analog input channels from either the LINE IN or MICROPHONE inputs of jack J1, digitizes the analog values, and sends the digital values to the FPGA as a serial bit stream. (There are two other analog input channels, INT0 and INT1, that are accessible only through header JP2.) The codec also accepts a serial bit stream from the FPGA and converts it into two analog output signals, which exit the XSB Board through the LINE OUT of J1. The serial bit streams are synchronized with a clock from the FPGA that enters the codec on the BCLK signal. The FPGA uses the LRCK signal to select the left or right channel as the source/destination of the serial data. The master clock from the FPGA (MCLK) synchronizes all the internal operations of the codec.

The audio codec has many programmable features that are configured through the CCLK, CDTI and CDTO pins. These pins are accessible through the Peripheral Bus. The chip-select of the audio codec (CSN#) is driven low when configuration data is to be loaded into the codec.

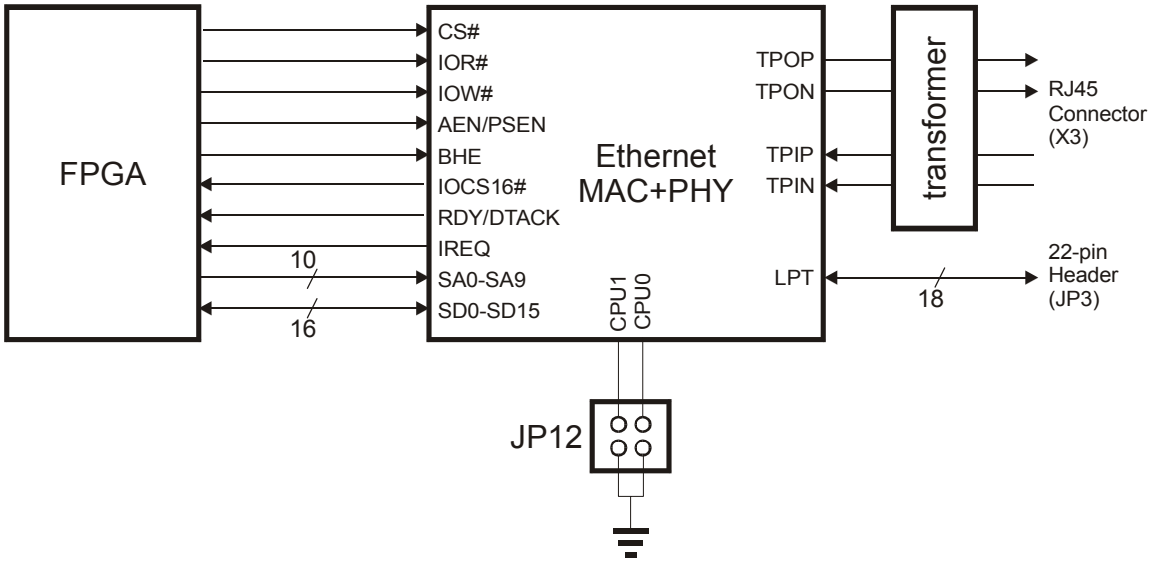


The FPGA pins which connect to the audio codec are as follows:

Peripheral Bus	Audio Bus	Codec Pin	FPGA Pin	Function
	AU-CSN#	CSN#	165	Audio codec chip-select (active-low)
PB-D0		CCLK	153	Configuration control clock
PB-D1		CDTI	145	Configuration data input
PB-D2		CDTO	141	Configuration data output
	AU-MCLK	MCLK	167	Master clock
	AU-LRCK	LRCK	168	Left/Right channel control
	AU-BCLK	BCLK	166	Serial data bit clock
	AU-SDTI	SDTI	169	Serial data input
	AU-SDTO0	SDTO0	173	Serial data output

10/100 Ethernet Interface

The XSB Board sends data over an Ethernet LAN at 10 or 100 Mbps through an Ethernet MAC+PHY chip (AX88796). The FPGA controls the Ethernet chip by reading and writing registers and FIFO buffers on the chip through a standard microprocessor bus interface.



The Ethernet chip supports several microprocessor bus interfaces. The interface is chosen by setting the shunts on jumper JP12 as follows:

Microprocessor Interface	JP12 Shunt Settings	
	CPU1	CPU0
MCS-51 (805X)	OFF	OFF
MC68K	OFF	ON
80186	ON	OFF
ISA Bus	ON	ON

The base address of the Ethernet chip is set by jumpers SJ1, SJ2 and SJ3. The default address is 0x200.

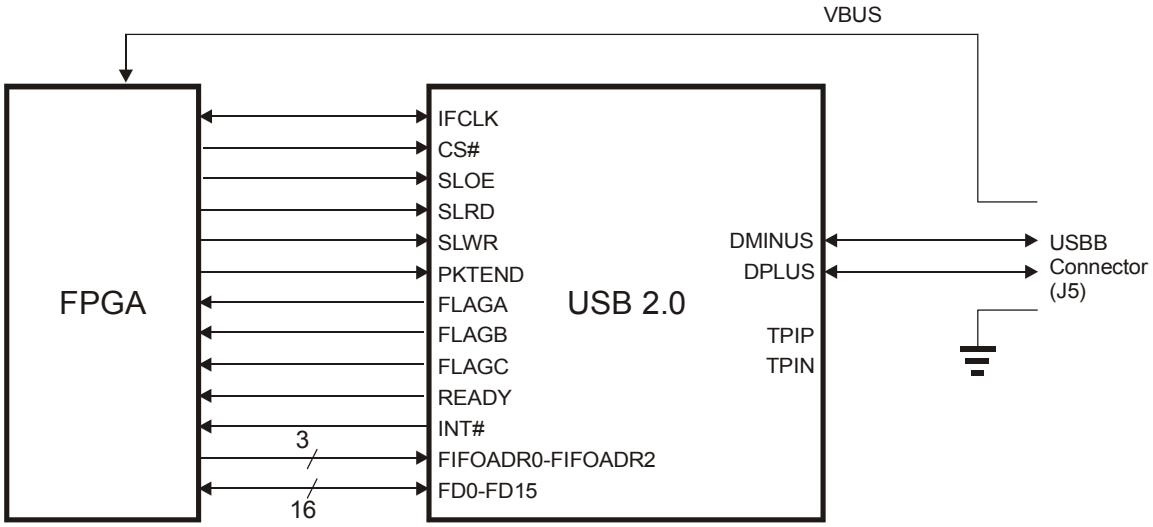
The Ethernet chip also has eighteen general-purpose I/O pins that can be accessed through I/O reads and writes. These I/O pins are brought out of the XSB Board though header JP3.

The connections of the Ethernet chip to the FPGA are listed below:

Peripheral Bus	Ethernet Bus	MAC+PHY Pin	FPGA Pin	Function
	ETHERNET-CS#	CS#	82	MAC+PHY chip-select
PB-OE#		IOR#	125	I/O read input (active-low)
PB-WE#		IOW#	123	I/O write input (active-low)
PB-LB#		AEN/PSEN	140	Address enable input
PB-UB#		BHE#	146	Enable the upper-byte of the databus (active-low)
	ETHERNET-IOCS16#	IOCS16#	74	Indicates an I/O address is 16-bits wide when this output is low
	ETHERNET-RDY/DTACK	RDY/DTACK	81	Insert a wait state during R/W operations when this output is low
	ETHERNET-IREQ	IREQ	75	Interrupt request output
PB-A0		SA0	83	MAC+PHY address line 0
PB-A1		SA1	84	MAC+PHY address line 1
PB-A2		SA2	86	MAC+PHY address line 2
PB-A3		SA3	87	MAC+PHY address line 3
PB-A4		SA4	88	MAC+PHY address line 4
PB-A5		SA5	89	MAC+PHY address line 5
PB-A6		SA6	93	MAC+PHY address line 6
PB-A7		SA7	94	MAC+PHY address line 7
PB-A8		SA8	100	MAC+PHY address line 8
PB-A9		SA9	101	MAC+PHY address line 9
PB-D0		SD0	153	MAC+PHY data line 0
PB-D1		SD1	145	MAC+PHY data line 1
PB-D2		SD2	141	MAC+PHY data line 2
PB-D3		SD3	135	MAC+PHY data line 3
PB-D4		SD4	126	MAC+PHY data line 4
PB-D5		SD5	120	MAC+PHY data line 5
PB-D6		SD6	116	MAC+PHY data line 6
PB-D7		SD7	108	MAC+PHY data line 7
PB-D8		SD8	127	MAC+PHY data line 8
PB-D9		SD9	129	MAC+PHY data line 9
PB-D10		SD10	132	MAC+PHY data line 10
PB-D11		SD11	133	MAC+PHY data line 11
PB-D12		SD12	134	MAC+PHY data line 12
PB-D13		SD13	136	MAC+PHY data line 13
PB-D14		SD14	138	MAC+PHY data line 14
PB-D15		SD15	139	MAC+PHY data line 15

USB 2.0 Interface

The XSB Board acts as a USB 2.0 peripheral through a USB chip (CY7C68001). The FPGA controls the USB chip by reading and writing registers and FIFO buffers on the chip through a microprocessor bus interface. The FPGA also has a direct connection to the VBUS signal of the USB connector so it can detect the presence of power on the USB bus. This is needed to determine whether it is allowable to connect to the USB bus or not.



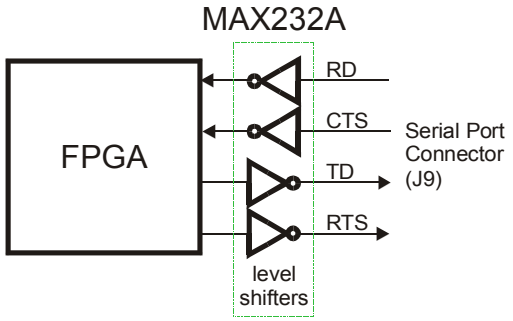
The connections of the USB chip to the FPGA are listed below:

Peripheral Bus	USB Bus	USB Chip Pin	FPGA Pin	Function
	USB-IFCLK	IFCLK	163	Input/output clock for the USB interface
	USB-CS#	CS#	148	USB interface chip-select
PB-OE#		SLOE	125	FIFO/command data bus output-enable
PB-A18		SLRD	121	FIFO/command read input
PB-A19		SLWR	122	FIFO/command write input
PB-A17		PKTEND	115	End-of-packet input
	USB-FLAGA	FLAGA	162	Programmable flag status output
	USB-FLAGB	FLAGB	152	FIFO full status output
	USB-FLAGC	FLAGC	151	FIFO empty status output
	USB-READY	READY	150	Insert a wait state during R/W operations
	USB-INT#	INT#	149	Interrupt request output
PB-A0		SA0	83	FIFO/command address line 0
PB-A1		SA1	84	FIFO/command address line 1
PB-A2		SA2	86	FIFO/command address line 2
PB-D0		SD0	153	FIFO/command data line 0
PB-D1		SD1	145	FIFO/command data line 1
PB-D2		SD2	141	FIFO/command data line 2
PB-D3		SD3	135	FIFO/command data line 3
PB-D4		SD4	126	FIFO/command data line 4
PB-D5		SD5	120	FIFO/command data line 5
PB-D6		SD6	116	FIFO/command data line 6
PB-D7		SD7	108	FIFO/command data line 7
PB-D8		SD8	127	FIFO/command data line 8
PB-D9		SD9	129	FIFO/command data line 9
PB-D10		SD10	132	FIFO/command data line 10
PB-D11		SD11	133	FIFO/command data line 11
PB-D12		SD12	134	FIFO/command data line 12
PB-D13		SD13	136	FIFO/command data line 13
PB-D14		SD14	138	FIFO/command data line 14
PB-D15		SD15	139	FIFO/command data line 15
	USB-VBUS	NC	164	USB power-sense

Serial Port

The FPGA handles the interface to the serial port. The four active lines of the serial port connect to the FPGA as follows.

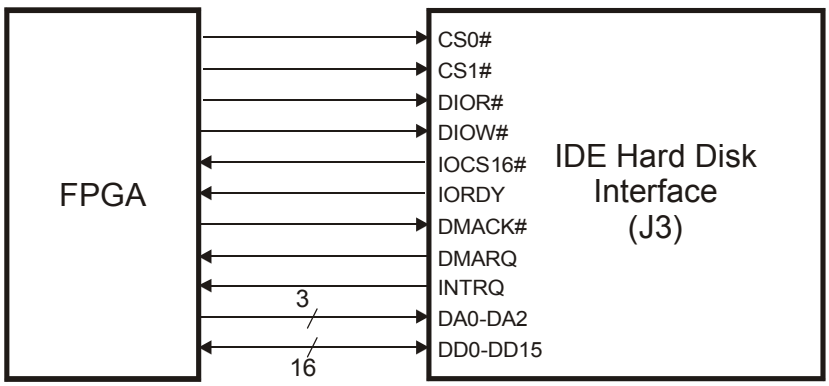
Serial Port Pin	FPGA Pin
RS232-RTS	70
RS232-TD	71
RS232-CTS	69
RS232-RD	73



IDE Hard Disk Interface

For nonvolatile data storage and retrieval, the XSB Board can access a hard disk through the IDE interface connector. The FPGA stores and retrieves data from the disk by reading and writing registers on the disk through the IDE interface. These registers are accessed using the read and write strobes in combination with the register bank select lines, the three-bit register address bus and the sixteen-bit data bus.

In addition to polled access, the IDE interface also allows DMA access using the DMA request and acknowledge signals along with the I/O ready signal.

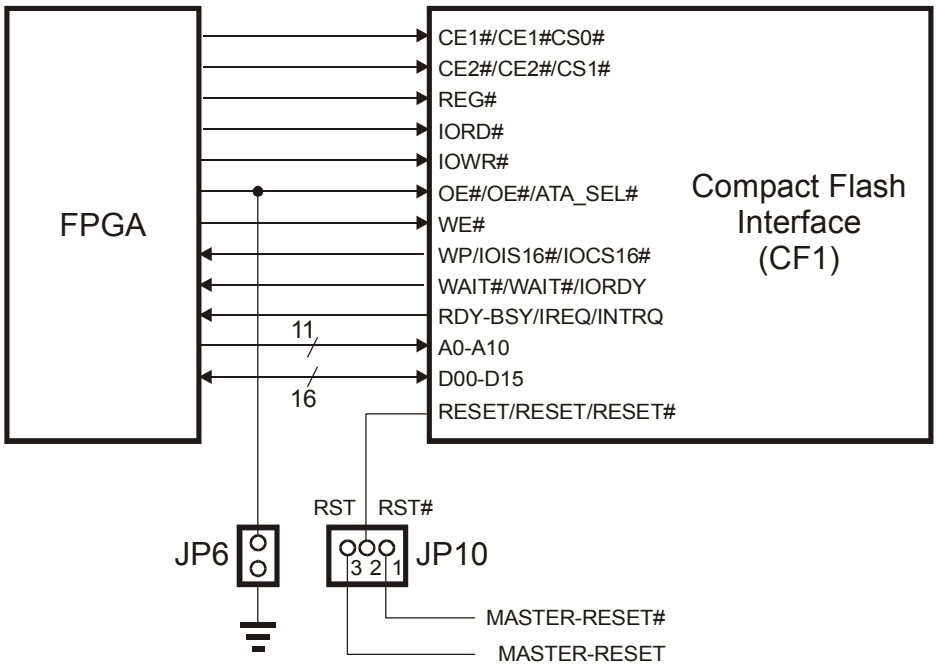


The connections between the IDE interface and the FPGA are listed below:

Peripheral Bus	Non-Volatile Bus	IDE Interface Pin	FPGA Pin	Function
	NV-CS0#	CS0#	59	IDE command block select (active-low)
	NV-CS1#	CS1#	60	IDE control block select (active-low)
PB-A18		DIOR#	121	I/O read input (active-low)
PB-A19		DIOW#	122	I/O write input (active-low)
	NV-IOCS16#	IOCS16#	63	Indicates 16-bit I/O is available
	NV-IORDY	IORDY	62	Insert a wait state during R/W operations
	NV-DMACK#	DMACK#	64	DMA acknowledge input (active-low)
	NV-DMARQ	DMARQ	68	DMA request output
	NV-INTRQ	INTRQ	61	Interrupt request output
PB-A0		DA0	83	IDE register address line 0
PB-A1		DA1	84	IDE register address line 1
PB-A2		DA2	86	IDE register address line 2
PB-D0		DD0	153	IDE data line 0
PB-D1		DD1	145	IDE data line 1
PB-D2		DD2	141	IDE data line 2
PB-D3		DD3	135	IDE data line 3
PB-D4		DD4	126	IDE data line 4
PB-D5		DD5	120	IDE data line 5
PB-D6		DD6	116	IDE data line 6
PB-D7		DD7	108	IDE data line 7
PB-D8		DD8	127	IDE data line 8
PB-D9		DD9	129	IDE data line 9
PB-D10		DD10	132	IDE data line 10
PB-D11		DD11	133	IDE data line 11
PB-D12		DD12	134	IDE data line 12
PB-D13		DD13	136	IDE data line 13
PB-D14		DD14	138	IDE data line 14
PB-D15		DD15	139	IDE data line 15

Compact Flash Interface

For nonvolatile data storage and retrieval, the XSB Board can access a Compact Flash card through the Compact Flash connector. The FPGA stores and retrieves data from the card by reading and writing registers on the card through the Compact Flash interface. When the card is used in True IDE mode, these registers are accessed in an identical fashion to those of an IDE hard disk. The interface also supports the use of Compact Flash cards in the memory or I/O modes.



Depending upon the mode in which the Compact Flash card is to be accessed, the shunts on jumpers JP6 and JP10 must be set as follows:

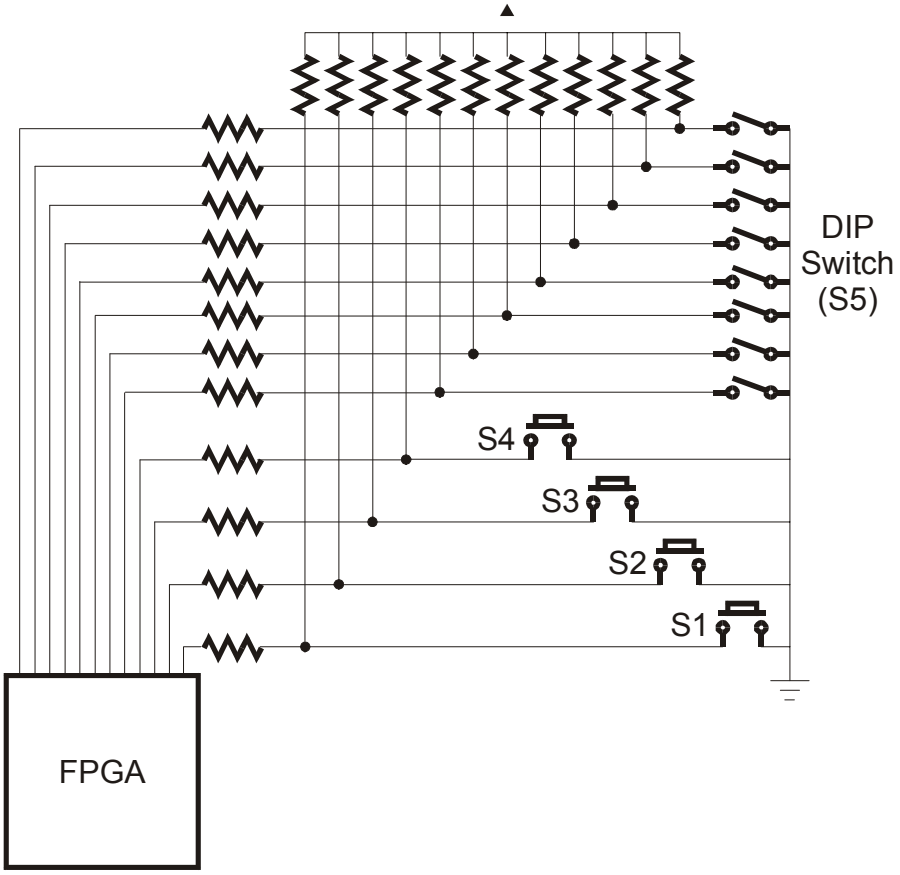
Compact Flash Card Mode	Shunt Settings	
	JP6	JP10
Memory	OFF	RST
I/O	OFF	RST
True IDE	ON	RST#

The connections between the Compact Flash interface and the FPGA are listed below:

Peripheral Bus	Non-Volatile Bus	Compact Flash Pin			FPGA Pin	Function
		MEM	I/O	True IDE		
	NV-CS0#	CE1#	CE1#	CS0#	59	chip-select (active-low)
	NV-CS1#	CE2#	CE2#	CS1#	60	chip-select (active-low)
PB-A17		REG#	REG#	REG#		register-select (active-low)
PB-A18		IORD#	IORD#	IORD#	121	I/O read input (active-low)
PB-A19		IOWR#	IOWR#	IOWR#	122	I/O write input (active-low)
PB-OE#		OE#	OE#	ATA_SEL#		memory & register output-enable
PB-WE#		WE#	WE#	WE#		memory & register write-enable
	NV-IOCS16#	WP	IOIS16#	IOCS16#	63	Indicates 16-bit I/O is available
	NV-IORDY	WAIT#	WAIT#	IORDY	62	Insert a wait state during R/W ops
	NV-INTRQ	RDY-BSY	IREQ	INTRQ	61	Interrupt request output
PB-A0				DA0	83	Compact Flash register address line 0
PB-A1				DA1	84	Compact Flash register address line 1
PB-A2				DA2	86	Compact Flash register address line 2
PB-A3				DA1	84	Compact Flash register address line 3
PB-A4				DA2	86	Compact Flash register address line 4
PB-A5				DA1	84	Compact Flash register address line 5
PB-A6				DA2	86	Compact Flash register address line 6
PB-A7				DA1	84	Compact Flash register address line 7
PB-A8				DA2	86	Compact Flash register address line 8
PB-A9				DA1	84	Compact Flash register address line 9
PB-A10				DA2	86	Compact Flash register address line 10
PB-D0				DD0	153	Compact Flash data line 0
PB-D1				DD1	145	Compact Flash data line 1
PB-D2				DD2	141	Compact Flash data line 2
PB-D3				DD3	135	Compact Flash data line 3
PB-D4				DD4	126	Compact Flash data line 4
PB-D5				DD5	120	Compact Flash data line 5
PB-D6				DD6	116	Compact Flash data line 6
PB-D7				DD7	108	Compact Flash data line 7
PB-D8				DD8	127	Compact Flash data line 8
PB-D9				DD9	129	Compact Flash data line 9
PB-D10				DD10	132	Compact Flash data line 10
PB-D11				DD11	133	Compact Flash data line 11
PB-D12				DD12	134	Compact Flash data line 12
PB-D13				DD13	136	Compact Flash data line 13
PB-D14				DD14	138	Compact Flash data line 14
PB-D15				DD15	139	Compact Flash data line 15

Pushbuttons and Eight-Position DIP Switch

The XSB Board has a bank of eight DIP switches and four pushbuttons that are accessible from the FPGA through the upper address lines of the Peripheral Bus. When pressed, each pushbutton pulls the connected pin of the FPGA to ground. Otherwise, the pin is pulled high through a resistor. Likewise, each DIP switch pulls the connected pin of the FPGA to ground when it is closed or ON. When the DIP switch is open or OFF, the pin is pulled high through a resistor. Current limiting resistors are placed in series with all the pushbuttons and switches so they do not affect the other components that drive the Peripheral Bus.

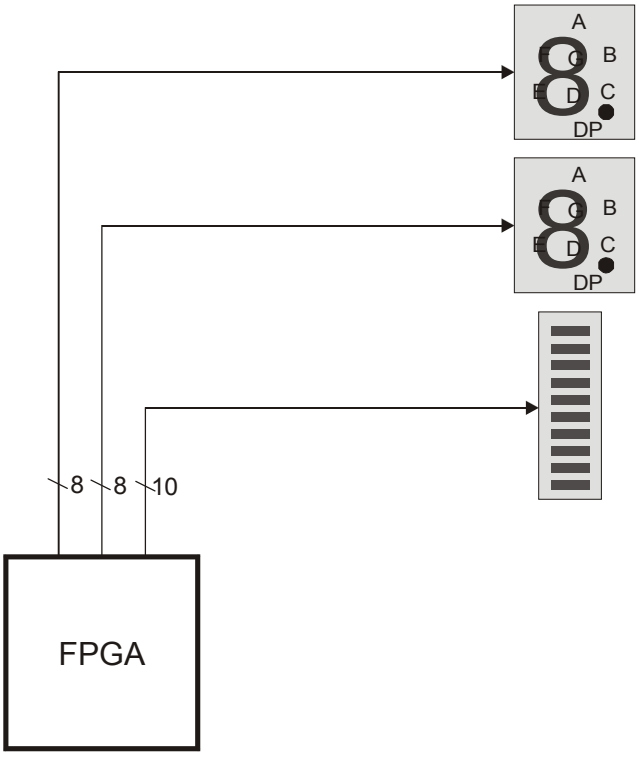


The table below lists the connections from the FPGA to the switches. The DIP switches also share the same pins as the uppermost eight bits of the Flash RAM address bus. If the Flash RAM is programmed with several FPGA bitstreams, then the DIP switch can be used to select a particular bitstreams which will be loaded into the FPGA by the CPLD on power-up.

Peripheral Bus	Switch	FPGA Pin	Function
PB-A8	S1	100	Pushbutton 1
PB-A9	S2	101	Pushbutton 2
PB-A10	S3		Pushbutton 3
PB-A11	S4	109	Pushbutton 4
PB-A12	S5-1	110	DIP switch 1
PB-A13	S5-2	111	DIP switch 2
PB-A14	S5-3	112	DIP switch 3
PB-A15	S5-4	113	DIP switch 4
PB-A16	S5-5	114	DIP switch 5
PB-A17	S5-6	115	DIP switch 6
PB-A18	S5-7	121	DIP switch 7
PB-A19	S5-8	122	DIP switch 8

Digit and Bargraph LEDs

The XSB Board has a 10-segment bargraph LED and two more 7-segment LED digits for use by the FPGA. All of these LEDs are active-high meaning that an LED segment will glow when a logic-high is applied to it.



The table below lists the connections from the FPGA to the LEDs. The LEDs are attached through the Peripheral Bus so the other components on the bus must be tristated if a stable display is desired.

Peripheral Bus	LED Segments		FPGA Pin	Function
PB-D0	LED1 (LEFT DIGIT)	A	153	
PB-D1		B	145	
PB-D2		C	141	
PB-D3		D	135	
PB-D4		E	126	
PB-D5		F	120	
PB-D6		G	116	
PB-D7		DP	108	
PB-D8	LED2 (RIGHT DIGIT)	A	127	
PB-D9		B	129	
PB-D10		C	132	
PB-D11		D	133	
PB-D12		E	134	
PB-D13		F	136	
PB-D14		G	138	
PB-D15		DP	139	
PB-A0	DZ1 (BARGRAPH)	B1	83	
PB-A1		B2	84	
PB-A2		B3	86	
PB-A3		B4	87	
PB-A4		B5	88	
PB-A5		B6	89	
PB-A6		B7	93	
PB-A7		B8	94	
PB-LB#		B9	140	
PB-UB#		B10	146	

Expansion Headers

The XSB Board has the following expansion headers that connect it to external systems:

Expansion Header	# I/O Pins	Description
JP3	18	General-purpose I/O connected to the Ethernet controller chip. The I/O is accessible by reading/writing registers through the FPGA interface to the Ethernet controller.
JP5	34	General-purpose I/O that shares the FPGA pins that drive the video DAC.
JP7	44	General-purpose I/O that shares the FPGA pins connected to the Peripheral Bus.

The JP3 expansion header connects to a set of general-purpose I/O pins of the Ethernet controller chip. The FPGA can access these pins by performing reads/writes to a register within the Ethernet controller via the Peripheral Bus.

The JP5 expansion header connects to the signals that pass from the FPGA to the video DAC. This header provides another external interface to the FPGA if the functions of the DAC are not needed. **Any signals passing through the JP5 expansion header must be 3.3V or less! The interface is not 5V tolerant! The FPGA will be damaged if signals exceeding 3.3V are applied to pins of JP5!**

Video Output Bus	JP5 Pin	FPGA Pin	Function
	1		+3.3V for use by external system
	2		+3.3V for use by external system
VIDOUT-VSYNC#	3	7	VGA vertical sync pulse (active-low)
VIDOUT-HSYNC#	4	8	VGA horizontal sync pulse (active-low)
VIDOUT-GY0	5	9	Pixel green component bit 0
VIDOUT-GY1	6	10	Pixel green component bit 1
VIDOUT-GY2	7	11	Pixel green component bit 2
VIDOUT-GY3	8	15	Pixel green component bit 3
VIDOUT-GY4	9	16	Pixel green component bit 4
VIDOUT-GY5	10	17	Pixel green component bit 5
VIDOUT-GY6	11	18	Pixel green component bit 6
VIDOUT-GY7	12	20	Pixel green component bit 7
VIDOUT-GY8	13	21	Pixel green component bit 8
VIDOUT-GY9	14	22	Pixel green component bit 9
VIDOUT-CLK	15	23	Pixel clock input
VIDOUT-BLANK#	16	24	Video blanking signal (active-low)
VIDOUT-RCR9	17	27	Pixel red component bit 9
VIDOUT-RCR8	18	29	Pixel red component bit 8
VIDOUT-RCR7	19	30	Pixel red component bit 7
VIDOUT-RCR6	20	31	Pixel red component bit 6
VIDOUT-RCR5	21	33	Pixel red component bit 5
VIDOUT-RCR4	22	34	Pixel red component bit 4
VIDOUT-RCR3	23	35	Pixel red component bit 3
VIDOUT-RCR2	24	36	Pixel red component bit 2
VIDOUT-RCR1	25	40	Pixel red component bit 1
VIDOUT-RCR0	26	41	Pixel red component bit 0
VIDOUT-BCB0	27	42	Pixel blue component bit 0
VIDOUT-BCB1	28	43	Pixel blue component bit 1
VIDOUT-BCB2	29	44	Pixel blue component bit 2
VIDOUT-BCB3	30	45	Pixel blue component bit 3
VIDOUT-BCB4	31	46	Pixel blue component bit 4
VIDOUT-BCB5	32	47	Pixel blue component bit 5
VIDOUT-BCB6	33	48	Pixel blue component bit 6
VIDOUT-BCB7	34	49	Pixel blue component bit 7
VIDOUT-BCB8	35	55	Pixel blue component bit 8
VIDOUT-BCB9	36	56	Pixel blue component bit 9
	37		Ground
	38		Ground

The JP7 expansion header connects to the signals of the Peripheral Bus. External chip-select signals are provided through this interface so that any external system can be tristated when the Peripheral Bus is being used by components on the XSB Board. **Any signals passing through the JP7 expansion header must be 3.3V or less! The interface is not 5V tolerant! The FPGA will be damaged if signals exceeding 3.3V are applied to pins of JP7!**

Peripheral Bus	Video Input Bus	JP7 Pin	FPGA Pin	Function
		1		+3.3V for use by external system
		2		+3.3V for use by external system
PB-OE#		3	125	Output-enable
PB-WE#		4	123	Write-enable
PB-LB#		5	140	Enable lower byte of data bus
PB-UB#		6	146	Enable upper byte of data bus
PB-D0		7	153	Data line 0
PB-D1		8	145	Data line 1
PB-D2		9	141	Data line 2
PB-D3		10	135	Data line 3
PB-D4		11	126	Data line 4
PB-D5		12	120	Data line 5
PB-D6		13	116	Data line 6
PB-D7		14	108	Data line 7
PB-D8		15	127	Data line 8
PB-D9		16	129	Data line 9
PB-D10		17	132	Data line 10
PB-D11		18	133	Data line 11
PB-D12		19	134	Data line 12
PB-D13		20	136	Data line 13
PB-D14		21	138	Data line 14
PB-D15		22	139	Data line 15
PB-A0		23	83	Address line 0
PB-A1		24	84	Address line 1
PB-A2		25	86	Address line 2
PB-A3		26	87	Address line 3
PB-A4		27	88	Address line 4
PB-A5		28	89	Address line 5
PB-A6		29	93	Address line 6
PB-A7		30	94	Address line 7
PB-A8		31	100	Address line 8
PB-A9		32	101	Address line 9
PB-A10		33	102	Address line 10
PB-A11		34	109	Address line 11
PB-A12		35	110	Address line 12

Peripheral Bus	Video Input Bus	JP7 Pin	FPGA Pin	Function
PB-A13		36	111	Address line 13
PB-A14		37	112	Address line 14
PB-A15		38	113	Address line 15
PB-A16		39	114	Address line 16
PB-A17		40	115	Address line 17
PB-A18		41	121	Address line 18
PB-A19		42	122	Address line 19
PB-ECS0#		43	58	External device chip-select 0
	VIDIN-HPD5	44	180	External device chip-select 1
	VIDIN-HPD6	45	181	External device chip-select 2
	VIDIN-HPD7	46	187	External device chip-select 3
		47		Ground
		48		Ground

Parallel Port Interface

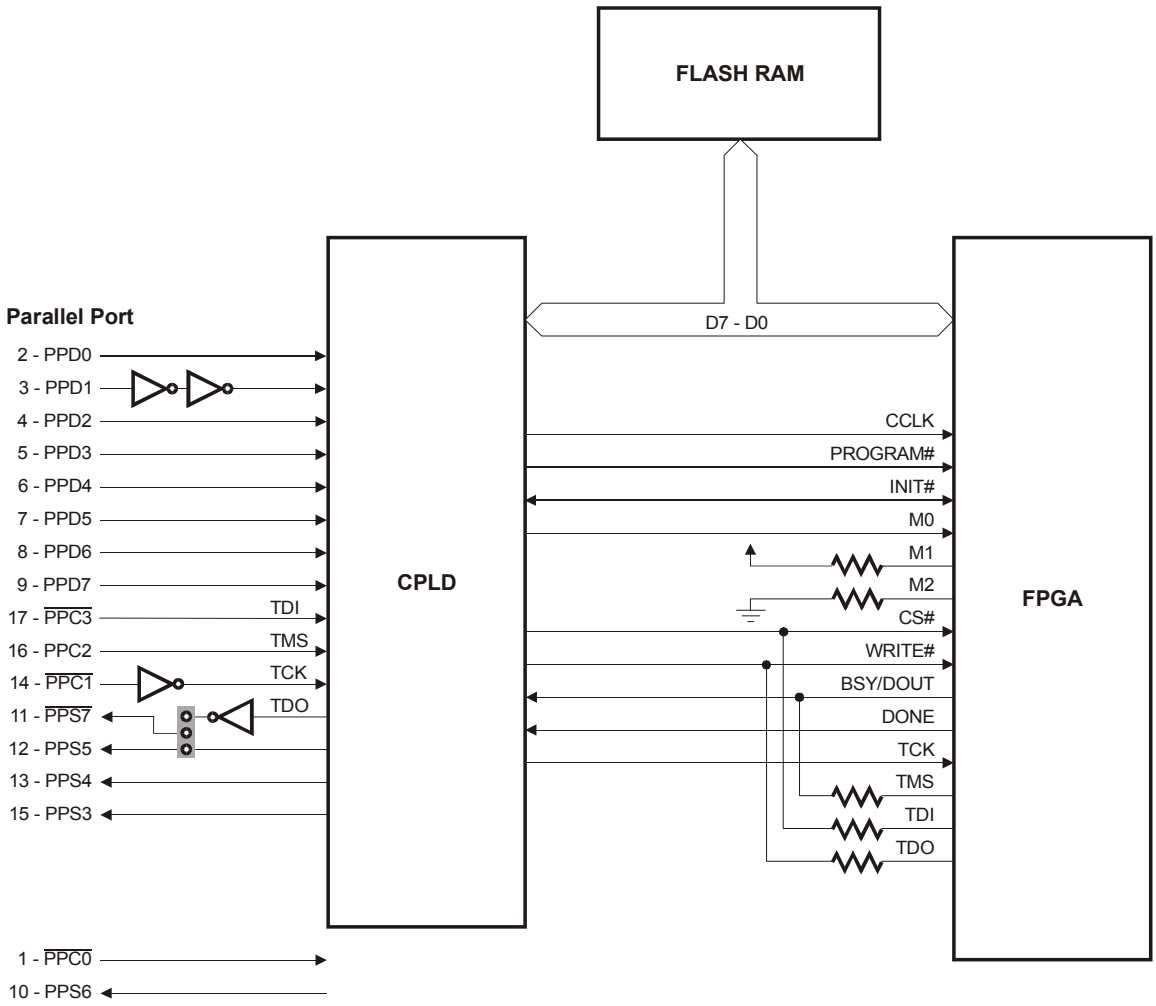
The parallel port is the main interface for communicating with the XSB Board. The CPLD handles fifteen lines of the parallel port interface (control signal C0 and status signal S6 are not used). Eleven of the active lines of the parallel port connect to general-purpose I/O pins on the CPLD.

Three of the parallel port control lines, C1–C3, connect to the JTAG pins through which the CPLD is programmed. The C1 control line clocks configuration data presented on the C3 line into the CPLD while the C2 signal steers the actions of the CPLD programming state machine. Meanwhile, information from the CPLD returns to the PC through status line S7.

The eight data lines, D0–D7, and the remaining three status lines, S3–S5, connect to general-purpose pins of the CPLD. The CPLD can be programmed to act as an interface between the FPGA and the parallel port (the dwnldpar.svf file is an example of such an interface). Schmitt-trigger inverters are inserted into the D1 line so it can carry a clean clock edge for use by any state machine programmed into the CPLD. The CPLD connects to the configuration pins of the Spartan-II FPGA so it can pass configuration bitstreams from the parallel port to the FPGA. The actual configuration data is presented on the to the FPGA on the same 8-bit bus that connects the CPLD, Flash, seven-segment LED and FPGA. The CPLD also drives the configuration pins (CCLK, PROGRAM#, CS#, and WRITE#) of the FPGA that control the loading of a bitstream. The CPLD uses the M0 input of the FPGA to select either the slave-serial or master-select configuration mode (M1 and M2 are already hard-wired to VCC and GND, respectively.) The CPLD can monitor the status of the bitstream download through the INIT#, DONE, and BSY/DOUT pins of the FPGA.

The CPLD also has access to the FPGA JTAG pins: TCK, TMS, TDI, TDO. The TMS, TDI, and TDO pins share the connections with the BSY/DOUT, CS#, and WRITE# pins. With these connections, the CPLD can be programmed with an interface that allows configuration of the Spartan-II FPGA through the Xilinx iMPACT or JTAG Programmer

software utilities. Jumper JP1 allows the connection of status pin S7 to the general-purpose CPLD pin that also drives status pin S5. This is needed to implement the parallel port interface required by the Xilinx software.



After the FPGA is configured with a bitstream and the DONE pin goes high, the CPLD switches into a mode that connects the parallel port data and status pins to the FPGA. For more details on how the CPLD manages the interface between the parallel port and the FPGA both before and after device configuration, see the XSB Parallel Port Interface application note.

Reset Circuitry

There are two reset pushbuttons on the XSB Board:

Reset Button	Function
RESET (S6)	Resets the audio codec, Ethernet controller, video decoder, USB chip, programmable oscillator, Compact Flash card and IDE disk.
PROG (S7)	Erases the current FPGA configuration.

Power Connectors

A standard ATX PC power supply can be connected to the XSB Board through connector J4. The connector is keyed so power cannot be applied with the wrong polarity. We recommend using the ATX power supply due to its stability and current capacity.

The XSB Board can also be powered from a 9V DC power supply through jack J2. The power supply must have a 2.1mm, center-positive plug. Three voltage regulators will generate the 5V, 3.3V and 1.8V voltages for the other XSB Board components. We do not recommend the 9V DC power input for general use!

A

XSB Pin Connections

The following tables list the pin numbers of the FPGA and CPLD along with the pin names of the other chips that they connect to. These connections correspond with the pin assignments in the user-constraint files FPGA.UCF and CPLD.UCF.

Connections Between the FPGA and Other XSB Board Components

FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
1	GND																			
2	TMS	FPGA-BSY/DOUT/TMS	18																	
3		ADC-CLK						CLK												
4		ADC-OE#						OE#												
5		I2C-SDA					SDA													SDAT
6		I2C-SCL					SCL													SCLK
7		VIDOUT-VSYNC#																3		
8		VIDOUT-HSYNC#																4		
9		VIDOUT-GY0							GY0									5		
10		VIDOUT-GY1							GY1									6		
11		VIDOUT-GY2							GY2									7		
12	GND																			
13	VCCO																			
14	VCCINT																			
15		VIDOUT-GY3							GY3									8		
16		VIDOUT-GY4							GY4									9		
17		VIDOUT-GY5							GY5									10		
18		VIDOUT-GY6							GY6									11		
19	GND																			
20		VIDOUT-GY7							GY7									12		
21		VIDOUT-GY8							GY8									13		
22		VIDOUT-GY9							GY9									14		
23		VIDOUT-CLK							CLK									15		
24		VIDOUT-BLANK#							BLANK#									16		
25	GND																			
26	VCCO																			
27		VIDOUT-RCR9							RCR9									17		
28	VCCINT																			
29		VIDOUT-RCR8							RCR8									18		
30		VIDOUT-RCR7							RCR7									19		
31		VIDOUT-RCR6							RCR6									20		
32	GND																			
33		VIDOUT-RCR5							RCR5									21		
34		VIDOUT-RCR4							RCR4									22		
35		VIDOUT-RCR3							RCR3									23		
36		VIDOUT-RCR2							RCR2									24		
37	VCCINT																			
38	VCCO																			
39	GND																			
40		VIDOUT-RCR1							RCR1									25		
41		VIDOUT-RCR0							RCR0									26		
42		VIDOUT-BCB0							BCB0									27		
43		VIDOUT-BCB1							BCB1									28		
44		VIDOUT-BCB2							BCB2									29		
45		VIDOUT-BCB3							BCB3									30		
46		VIDOUT-BCB4							BCB4									31		
47		VIDOUT-BCB5							BCB5									32		
48		VIDOUT-BCB6							BCB6									33		
49		VIDOUT-BCB7							BCB7									34		
50	M1	FPGA-M1(+3.3V)																		
51	GND																			
52	M0	FPGA-M0	36																	
53	VCCO																			
54	M2	FPGA-M2(GND)																		
55		VIDOUT-BCB8																35		
56		VIDOUT-BCB9																36		
57		FLASH-CE#	11	CE#																
58		PB-ECS0#																	43	
59		NV-CS0#												CS0#	CE1#/CE1#/CS0#					
60		NV-CS1#												CS1#	CE2#/CE2#/CS1#					
61		NV-INTRQ												INTRQ	RDY-BSY/IREQ/INTRQ					
62		NV-IORDY												IORDY	WAIT#/WAIT#/IORDY					
63		NV-IOCS16												IOCS16#	WP/IOIS16#/IOCS16#					
64		NV-DMACK#												DMACK#						
65	GND																			
66	VCCO																			
67	VCCINT																			
68		NV-DMARQ												DMARQ						
69		RS232-CTS														CTS				
70		RS232-RTS														RTS				
71		RS232-TD														TD				

Connections Between the FPGA and Other XSB Board Components																				
FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
72	GND																			
73		RS232-RD														RD				
74		ETHERNET-IOCS16#									IOCS16#									
75		ETHERNET-IREQ									IREQ									
76	VCCINT																			
77	I/GCK1	FPGA-CLK1																		CLKD
78	VCCO																			
79	GND																			
80	I/GCK0	SDRAM-CLK																		CLKB
81		ETHERNET-RDY/DTACK									RDY/DTACK									
82		ETHERNET-CS#									CS#									
83		PB-A0	1	A0	A0	A0					SA0	FIFOADR0		DA0	A00		BAR1		23	
84		PB-A1	64	A1	A1	A1					SA1	FIFOADR1		DA1	A01		BAR2		24	
85	GND																			
86		PB-A2	63	A2	A2	A2					SA2	FIFOADR2		DA2	A02		BAR3		25	
87		PB-A3	62	A3	A3	A3					SA3				A03		BAR4		26	
88		PB-A4	61	A4	A4	A4					SA4				A04		BAR5		27	
89		PB-A5	60	A5	A5	A5					SA5				A05		BAR6		28	
90	VCCINT																			
91	VCCO																			
92	GND																			
93		PB-A6	59	A6	A6	A6					SA6				A06		BAR7		29	
94		PB-A7	58	A7	A7	A7					SA7				A07		BAR8		30	
95		SDRAM-WE#				WE#														
96		SDRAM-CAS#				CAS#														
97		SDRAM-RAS#				RAS#														
98		SDRAM-CE#				CE#														
99		SDRAM-CKE				CKE														
100		PB-A8	45	A8	A8	A8					SA8				A08	S1			31	
101		PB-A9	44	A9	A9	A9					SA9				A09	S2			32	
102		PB-A10	57	A10	A10	A10									A10	S3			33	
103	GND																			
104	DONE	FPGA-DONE	40																	
105	VCCO																			
106	PROGRAM#	FPGA-PROGRAM#	39													S7				
107	INIT#	FPGA-INIT#	38																	
108	D7	PB-D7	10	D7	D7	D7					D7	FD7		DD7	D07		LEFT-DP		14	
109		PB-A11	43	A11	A11	A11										S4			34	
110		PB-A12	56	A12	A12	A12										S5-1			35	
111		PB-A13	46	A13	A13	BA0										S5-2			36	
112		PB-A14	47	A14	A14	BA1										S5-3			37	
113		PB-A15	52	A15	A15											S5-4			38	
114		PB-A16	51	A16	A16											S5-5			39	
115		PB-A17	48	A17	A17							PKTEND			REG#	S5-6			40	
116	D6	PB-D6	9	D6	D6	D6					D6	FD6		DD6	D06		LEFT-G		13	
117	GND																			
118	VCCO																			
119	VCCINT																			
120	D5	PB-D5	8	D5	D5	D5					D5	FD5		DD5	D05		LEFT-F		12	
121		PB-A18	42	A18								SLRD		DIOR#	IORD#	S5-7			41	
122		PB-A19	50									SLWR		DIOW#	IOWR#	S5-8			42	
123		PB-WE#	49	WE#	WE#						IOWR#				WE#				4	
124	GND																			
125		PB-OE#	12	OE#	OE#						IORD#	SLOE			OE#/OE#/ATA_SEL#				3	
126	D4	PB-D4	7	D4	D4	D4					D4	FD4		DD4	D04		LEFT-E		11	
127		PB-D8			D8	D8					D8	FD8		DD8	D08		RIGHT-A		15	
128	VCCINT																			
129		PB-D9			D9	D9					D9	FD9		DD9	D09		RIGHT-B		16	
130	VCCO																			
131	GND																			
132		PB-D10			D10	D10					D10	FD10		DD10	D10		RIGHT-C		17	
133		PB-D11			D11	D11					D11	FD11		DD11	D11		RIGHT-D		18	
134		PB-D12			D12	D12					D12	FD12		DD12	D12		RIGHT-E		19	
135	D3	PB-D3	6	D3	D3	D3					D3	FD3		DD3	D03		LEFT-D		10	
136		PB-D13			D13	D13					D13	FD13		DD13	D13		RIGHT-F		20	
137	GND																			
138		PB-D14			D14	D14					D14	FD14		DD14	D14		RIGHT-G		21	
139		PB-D15			D15	D15					D15	FD15		DD15	D15		RIGHT-DP		22	
140		PB-LB#			LB#	LDQM					AEN/PSEN						BAR9		5	
141	D2	PB-D2	5	D2	D2	D2				CDTO	D2	FD2		DD2	D02		LEFT-C		9	
142	VCCINT																			

Connections Between the FPGA and Other XSB Board Components																				
FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
143	VCCO																			
144	GND																			
145	D1	PB-D1	4	D1	D1	D1				CDTI	D1	FD1		DD1	D01		LEFT-B		8	
146		PB-UB#			UB#	UDQM					BHE#						BAR10		6	
147		RAM-CE#			CE#															
148		USB-CS#										CS#								
149		USB-INT#										INT#								
150		USB-READY										READY								
151		USB-FLAGC										FLAGC								
152		USB-FLAGB										FLAGB								
153	DIN/D0	PB-D0	2	D0	D0	D0				CCLK	D0	FD0		DD0	D00		LEFT-A		7	
154	DOUT/BUSY	FPGA-BSY/DOUT/TMS	18																	
155	CCLK	FPGA-CCLK	16																	
156	VCCO																			
157	TDO	FPGA-WRITE#/TDO	19																	
158	GND																			
159	TDI	FPGA-CS#/TDI	15																	
160	CS#	FPGA-CS#/TDI	15																	
161	WRITE#	FPGA-WRITE#/TDO	19																	
162		USB-FLAGA										FLAGA								
163		USB-IFCLK										IFCLK								
164		USB-VBUS																		
165		AU-CSN#								CSN#										
166		AU-BCLK								BCLK										
167		AU-MCLK								MCLK										
168		AU-LRCK								LRCK										
169		AU-SDTI								SDTI										
170	GND																			
171	VCCO																			
172	VCCINT																			
173		AU-SDTO0								SDTO0										
174		VIDIN-HPD0					HPD0	D8												
175		VIDIN-HPD1					HPD1	D9												
176		VIDIN-HPD2					HPD2	D10												
177	GND																			
178		VIDIN-HPD3					HPD3	D11												
179		VIDIN-HPD4					HPD4	OVRNG												
180		VIDIN-HPD5					HPD5												44	
181		VIDIN-HPD6					HPD6												45	
182	I/GCK2	FPGA-CLK0																		CLKC
183	GND																			
184	VCCO																			
185	I/GCK3	VIDIN-ICLK					ICLK													
186	VCCINT																			
187		VIDIN-HPD7					HPD7												46	
188		VIDIN-IPD0					IPD0	D0												
189		VIDIN-IPD1					IPD1	D1												
190	GND																			
191		VIDIN-IPD2					IPD2	D2												
192		VIDIN-IPD3					IPD3	D3												
193		VIDIN-IPD4					IPD4	D4												
194		VIDIN-IPD5					IPD5	D5												
195	VCCINT																			
196	VCCO																			
197	GND																			
198		VIDIN-IPD6					IPD6	D6												
199		VIDIN-IPD7					IPD7	D7												
200		VIDIN-IGPH					IGPH													
201		VIDIN-IGPV					IGPV													
202		VIDIN-IGP1					IGP1													
203		VIDIN-IGP0					IGP0													
204		VIDIN-ITRI					ITRI													
205		VIDIN-IDQ					IDQ													
206		VIDIN-ITRDY					ITRDY													
207	TCK	FPGA-TCK	13																	
208	VCCO																			

Connections Between the CPLD and Other XSB Board Components

CPLD Pin	CPLD Pin Function	Net Name	FPGA Pin	Parallel Port	Flash	SRAM	SDRAM	Stereo Codec	Ether-net	USB	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP7	Prog. Osc.
1		PB-A0	83		A0	A0	A0		SA0	FIFOADR0	DA0	A00		BAR1	23	
2		PB-D0	153		D0	D0	D0	CCLK	D0	FD0	DD0	D00		LEFT-A	7	
3	VCCINT															
4		PB-D1	145		D1	D1	D1	CDTI	D1	FD1	DD1	D01		LEFT-B	8	
5		PB-D2	141		D2	D2	D2	CDTO	D2	FD2	DD2	D02		LEFT-C	9	
6		PB-D3	135		D3	D3	D3		D3	FD3	DD3	D03		LEFT-D	10	
7		PB-D4	126		D4	D4	D4		D4	FD4	DD4	D04		LEFT-E	11	
8		PB-D5	120		D5	D5	D5		D5	FD5	DD5	D05		LEFT-F	12	
9		PB-D6	116		D6	D6	D6		D6	FD6	DD6	D06		LEFT-G	13	
10		PB-D7	108		D7	D7	D7		D7	FD7	DD7	D07		LEFT-DP	14	
11		FLASH-CE#	57		CE#											
12		PB-OE#	125		OE#	OE#	OE#		IORD#	SLOE		OE#/OE#/ATA_SEL#			3	
13		FPGA-TCK	207													
14	GND															
15	GCK1	FPGA-CS#/TDI	159													
15	GCK1	FPGA-CS#/TDI	160													
16	GCK2	FPGA-CCLK	155													
17	GCK3	CPLD-CLK														XBUF
18		FPGA-BSY/DOUT/TMS	2													
18		FPGA-BSY/DOUT/TMS	154													
19		FPGA-WRITE#/TDO	157													
19		FPGA-WRITE#/TDO	161													
20		PP-S4		S4												
21	GND															
22		PP-D7		D7												
23		PP-D6		D6												
24		PP-D5		D5												
25		PP-D4		D4												
26	VCCIO															
27		PP-D3		D3												
28	TDI	PP-C3		C3												
29	TMS	PP-C2		C2												
30	TCK	PP-C1#		C1#												
31		PP-D2		D2												
32		PP-D1		D1												
33		PP-D0		D0												
34		PP-S3		S3												
35		PP-S5		S5												
36		FPGA-M0	52													
37	VCCINT															
38		FPGA-INIT#	107													
39		FPGA-PROGRAM#	106										S7			
40		FPGA-DONE	104													
41	GND															
42		PB-A18	121		A18					SLRD	DIOR#	IORD#	S5-7		41	
43		PB-A11	109		A11	A11	A11						S4		34	
44		PB-A9	101		A9	A9	A9		SA9			A09	S2		32	
45		PB-A8	100		A8	A8	A8		SA8			A08	S1		31	
46		PB-A13	111		A13	A13	BA0						S5-2		36	
47		PB-A14	112		A14	A14	BA1						S5-3		37	
48		PB-A17	115		A17	A17				PKTEND		REG#	S5-6		40	
49		PB-WE#	123		WE#	WE#	WE#		IOWR#			WE#			4	
50		PB-A19	122							SLWR	DIOW#	IOWR#	S5-8		42	
51		PB-A16	114		A16	A16							S5-5		39	
52		PB-A15	113		A15	A15							S5-4		38	
53	TDO			S7#												
54	GND															
55	VCCIO															
56		PB-A12	110		A12	A12	A12						S5-1		35	
57		PB-A10	102		A10	A10	A10					A10	S3		33	
58		PB-A7	94		A7	A7	A7		SA7			A07		BAR8	30	
59		PB-A6	93		A6	A6	A6		SA6			A06		BAR7	29	
60		PB-A5	89		A5	A5	A5		SA5			A05		BAR6	28	
61		PB-A4	88		A4	A4	A4		SA4			A04		BAR5	27	
62		PB-A3	87		A3	A3	A3		SA3			A03		BAR4	26	
63		PB-A2	86		A2	A2	A2		SA2	FIFOADR2	DA2	A02		BAR3	25	
64		PB-A1	84		A1	A1	A1		SA1	FIFOADR1	DA1	A01		BAR2	24	

B

XSB Schematics

The following pages show the detailed schematics for the XSB Board.


U1B7
ADC-CLK
ADC-OE#
I2C-SDA
I2C-SCL
VIDOUT-VSYNC#
VIDOUT-HSYNC#
VIDOUT-GY0
VIDOUT-GY1
VIDOUT-GY2
VIDOUT-GY3
VIDOUT-GY4
VIDOUT-GY5
VIDOUT-GY6
VIDOUT-GY7
VIDOUT-GY8
VIDOUT-GY9
VIDOUT-CLK
VIDOUT-BLANK#
IO_B7_0
IO_B7_1
IO_B7_2
IO_B7_3_(VREF,L49P)
IO_B7_4_(L49N)
IO_B7_5
IO_B7_6
IO_B7_7_(L48P)
IO_B7_8_(L48N)
IO_B7_9_(L47P_YY)
IO_B7_10_(L47N_YY)
IO_B7_11_(L46P_YY)
IO_B7_12_(L46N_YY)
IO_B7_13_(VREF,L45P)
IO_B7_14_(L45N)
IO_B7_15
IO_B7_16_(L44P_YY)
IO_B7_17_(IRDY,L44N_YY)
R52F 33
XC2S300E_PQ208
U1B6
VIDOUT-RCR9
VIDOUT-RCR8
VIDOUT-RCR7
VIDOUT-RCR6
VIDOUT-RCR5
VIDOUT-RCR4
VIDOUT-RCR3
VIDOUT-RCR2
VIDOUT-RCR1
VIDOUT-RCR0
VIDOUT-BCB0
VIDOUT-BCB1
VIDOUT-BCB2
VIDOUT-BCB3
VIDOUT-BCB4
VIDOUT-BCB5
VIDOUT-BCB6
VIDOUT-BCB7
IO_B6_0_(TRDY)
IO_B6_1
IO_B6_2_(L43P)
IO_B6_3_(VREF,L43N)
IO_B6_4_(L42P_YY)
IO_B6_5_(L42N_YY)
IO_B6_6_(L41P_YY)
IO_B6_7_(L41N_YY)
IO_B6_8_(L40P)
IO_B6_9_(L40N)
IO_B6_10
IO_B6_11
IO_B6_12
IO_B6_13_(VREF,L39P)
IO_B6_14_(L39N)
IO_B6_15
IO_B6_16_(L38P_YY)
IO_B6_17_(L38N_YY)
R54H 33
XC2S300E_PQ208
U1B5
VIDOUT-BCB8
VIDOUT-BCB9
FLASH-CE#
PB-ECS0#
NV-CS0#
NV-CS1#
NV-INTRQ
NV-IORDY
NV-IOCS16
NV-DMACK#
NV-DMARQ
RS232-CTS
RS232-RTS
RS232-TD
RS232-RD
ETHERNET-IOCS16#
ETHERNET-IREQ
IO_B5_0_(L37N_YY)
IO_B5_1_(L37P_YY)
IO_B5_2
IO_B5_3
IO_B5_4_(VREF,L36N_YY)
IO_B5_5_(L36P_YY)
IO_B5_6_(L35N)
IO_B5_7_(L35P)
IO_B5_8_(L34N)
IO_B5_9_(L34P)
IO_B5_10_(L33N)
IO_B5_11_(L33P)
IO_B5_12
IO_B5_13_(L32N)
IO_B5_14_(VREF,L32P)
IO_B5_15
IO_B5_16_(DLL,L31N)
XC2S300E_PQ208
+3.3V
R70A 4.7K
U1B4
ETHERNET-RDY/DTACK
ETHERNET-CS#
PB-A0
PB-A1
PB-A2
PB-A3
PB-A4
PB-A5
PB-A6
PB-A7
SDRAM-WE#
SDRAM-CAS#
SDRAM-RAS#
SDRAM-CE#
SDRAM-CKE
PB-A8
PB-A9
PB-A10
IO_B4_0_(DLL,L31P)
IO_B4_1
IO_B4_2_(L30N)
IO_B4_3_(VREF,L30P)
IO_B4_4_(L29N)
IO_B4_5_(L29P)
IO_B4_6_(L28N)
IO_B4_7_(L28P)
IO_B4_8_(L27N_YY)
IO_B4_9_(L27P_YY)
IO_B4_10
IO_B4_11
IO_B4_12_(L26N_YY)
IO_B4_13_(VREF,L26P_YY)
IO_B4_14
IO_B4_15
IO_B4_16_(L25N_YY)
IO_B4_17_(L25P_YY)
R52H 33
R58C 33
XC2S300E_PQ208
U1B3
FPGA-INIT#
PB-D7
PB-A11
PB-A12
PB-A13
PB-A14
PB-A15
PB-A16
PB-A17
PB-D6
PB-D5
PB-A18
PB-A19
PB-WE#
PB-OE#
PB-D4
PB-D8
PB-D9
IO_B3_0_(INIT#,L24N_YY)
IO_B3_1_(D7,L24P_YY)
IO_B3_2
IO_B3_3
IO_B3_4_(VREF,L23N)
IO_B3_5_(L23P)
IO_B3_6
IO_B3_7
IO_B3_8_(L22N)
IO_B3_9_(D6,L22P)
IO_B3_10_(D5,L21N_YY)
IO_B3_11_(L21P_YY)
IO_B3_12_(L20N_YY)
IO_B3_13_(L20P_YY)
IO_B3_14_(VREF,L19N)
IO_B3_15_(D4,L19P)
IO_B3_16
IO_B3_17_(TRDY)
R60D 33
XC2S300E_PQ208
U1B2
PB-D10
PB-D11
PB-D12
PB-D3
PB-D13
PB-D14
PB-D15
PB-LB#
PB-D2
PB-D1
PB-UB#
RAM-CE#
USB-CS#
USB-INT#
USB-READY
USB-FLAGC
USB-FLAGB
PB-D0
FPGA-BSY/DOUT/TMS
IO_B2_0_(IRDY,L18N_YY)
IO_B2_1_(L18P_YY)
IO_B2_2
IO_B2_3_(D3,L17N)
IO_B2_4_(VREF,L17P)
IO_B2_5_(L16N_YY)
IO_B2_6_(L16P_YY)
IO_B2_7_(L15N_YY)
IO_B2_8_(D2,L15P_YY)
IO_B2_9_(D1,L14N)
IO_B2_10_(L14P)
IO_B2_11
IO_B2_12
IO_B2_13
IO_B2_14_(VREF,L13N)
IO_B2_15_(L13P)
IO_B2_16
IO_B2_17_(DIN/D0,L12N_YY)
IO_B2_18_(DOUT/BUSY,L12P_YY)
R61H 33
XC2S300E_PQ208
+3.3V
+3.3V
R70C 4.7K
R70B 4.7K
U1CONFIG
FPGA-DONE
FPGA-PROGRAM#
FPGA-CCLK
FPGA-M0
+3.3V
GND
FPGA-TCK
FPGA-BSY/DOUT/TMS
FPGA-CS#/TDI
FPGA-WRITE#/TDO
SDRAM-CLK
FPGA-CLK1
FPGA-CLK0
VIDIN-ICLK
DONE
PROGRAM#
CCLK
M0
M1
M2
TCK
TMS
TDI
TDO
I/GCK0
I/GCK1
I/GCK2
I/GCK3
R69B 330
XC2S300E_PQ208
U1B1
FPGA-CS#/TDI
FPGA-WRITE#/TDO
USB-FLAGA
USB-IFCLK
USB-VBUS
AU-CSN#
AU-BCLK
AU-MCLK
AU-LRCK
AU-SDTI
AU-SDTO0
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
VIDIN-HPD5
VIDIN-HPD6
IO_B1_0_(CS#,L11P_YY)
IO_B1_1_(WRITE#,L11N_YY)
IO_B1_2
IO_B1_3
IO_B1_4_(VREF,L10P_YY)
IO_B1_5_(L10N_YY)
IO_B1_6
IO_B1_7
IO_B1_8_(L9P)
IO_B1_9_(L9N)
IO_B1_10_(L8P)
IO_B1_11_(L8N)
IO_B1_12_(L7P)
IO_B1_13_(L7N)
IO_B1_14_(VREF,L6P)
IO_B1_15_(L6N)
IO_B1_16
IO_B1_17_(DLL,L5N)
XC2S300E_PQ208
U1B0
VIDIN-HPD7
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-IGPH
VIDIN-IGPV
VIDIN-IGP1
VIDIN-IGP0
VIDIN-ITRI
VIDIN-IDQ
VIDIN-ITRDY
IO_B0_0_(DLL,L5N)
IO_B0_1_(L4P)
IO_B0_2_(VREF,L4N)
IO_B0_3_(L3P)
IO_B0_4_(L3N)
IO_B0_5_(L2P)
IO_B0_6_(L2N)
IO_B0_7_(L1P_YY)
IO_B0_8_(L1N_YY)
IO_B0_9
IO_B0_10
IO_B0_11_(L0P_YY)
IO_B0_12_(VREF,L0N_YY)
IO_B0_13
IO_B0_14
IO_B0_15
XC2S300E_PQ208
R70D 4.7K
R69D 330
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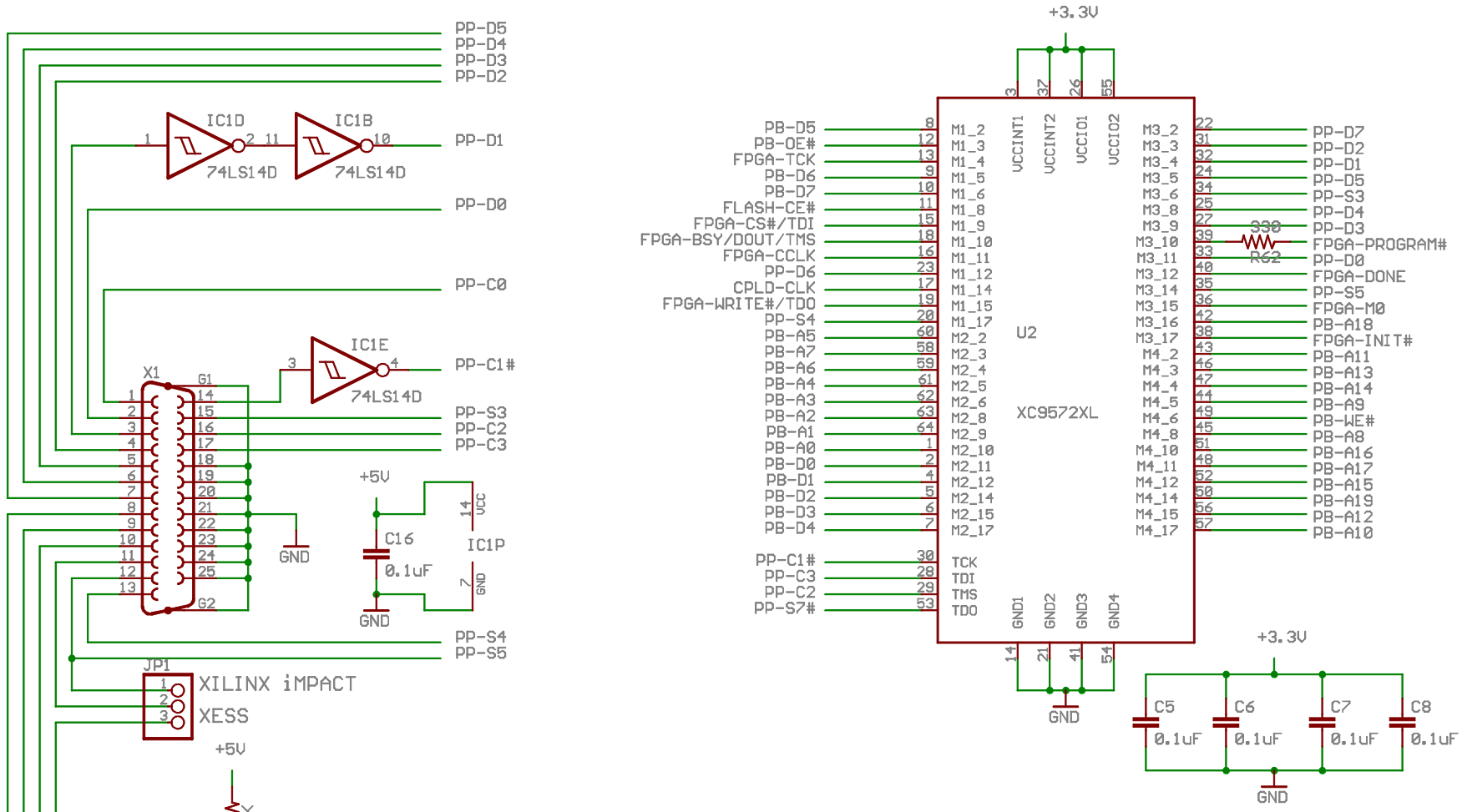

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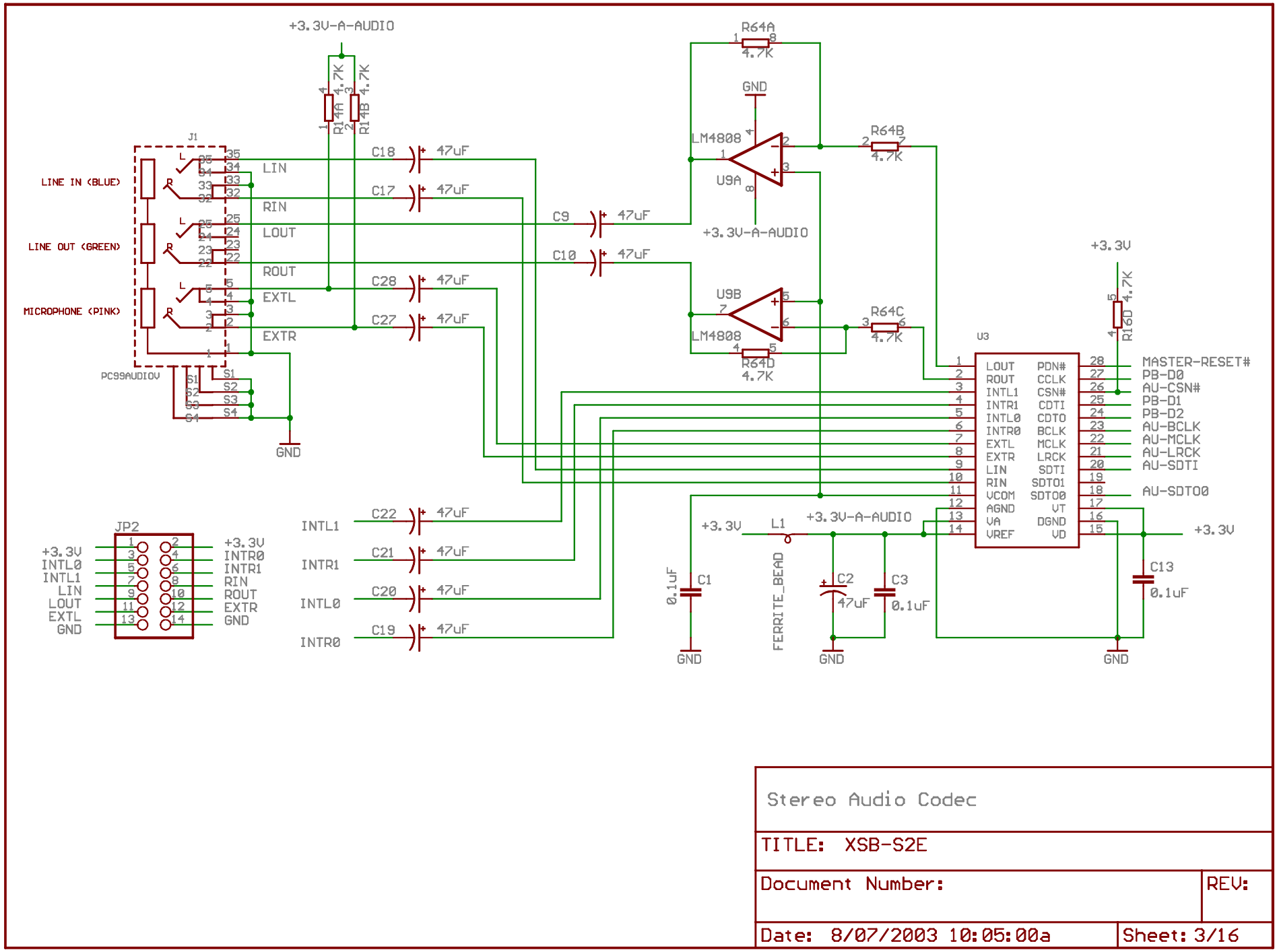

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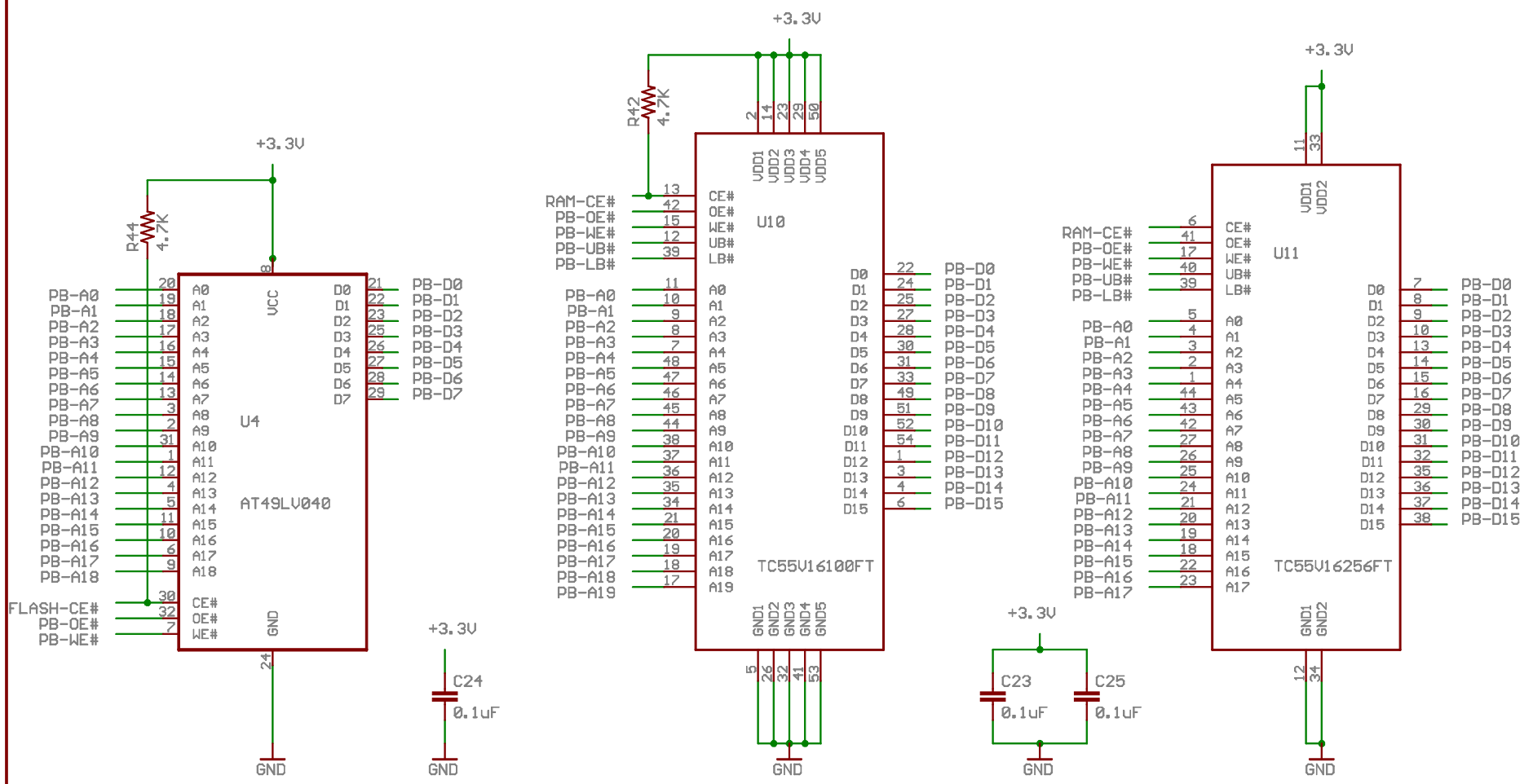

Flash and Static RAMs

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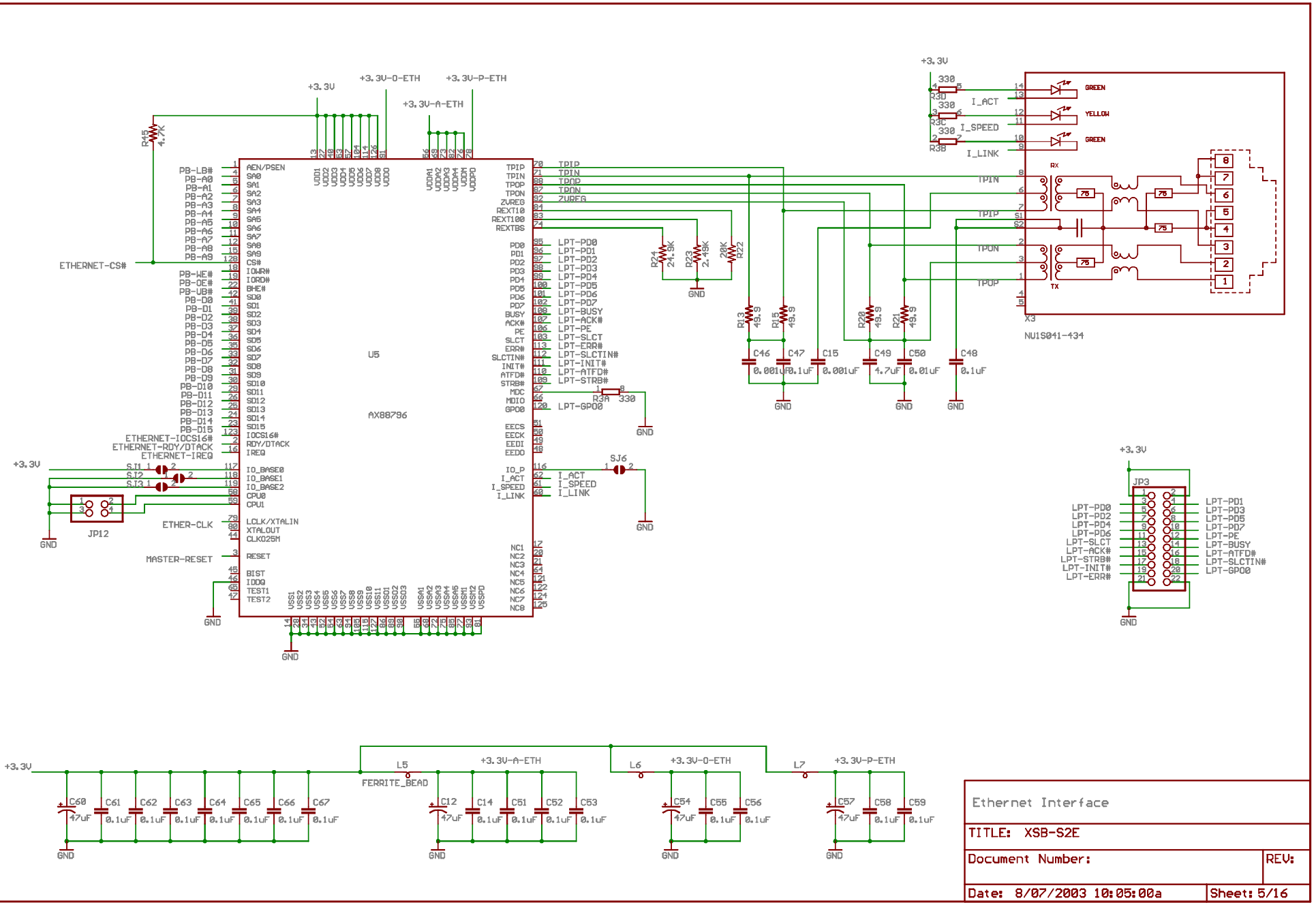

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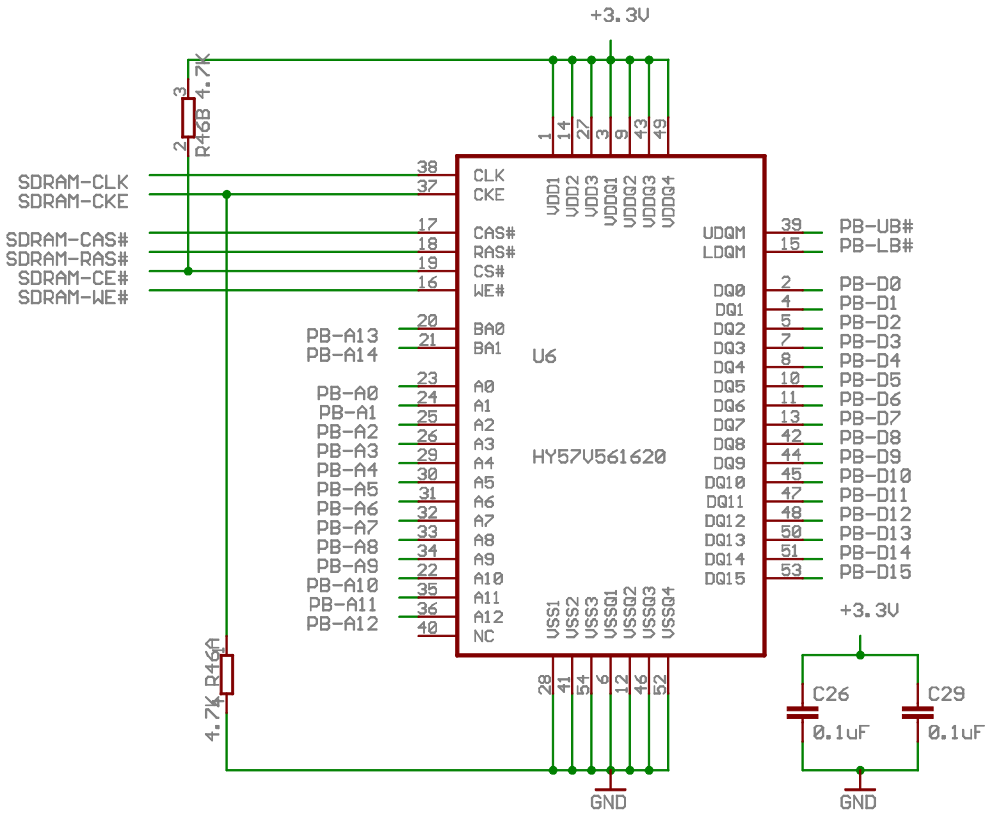

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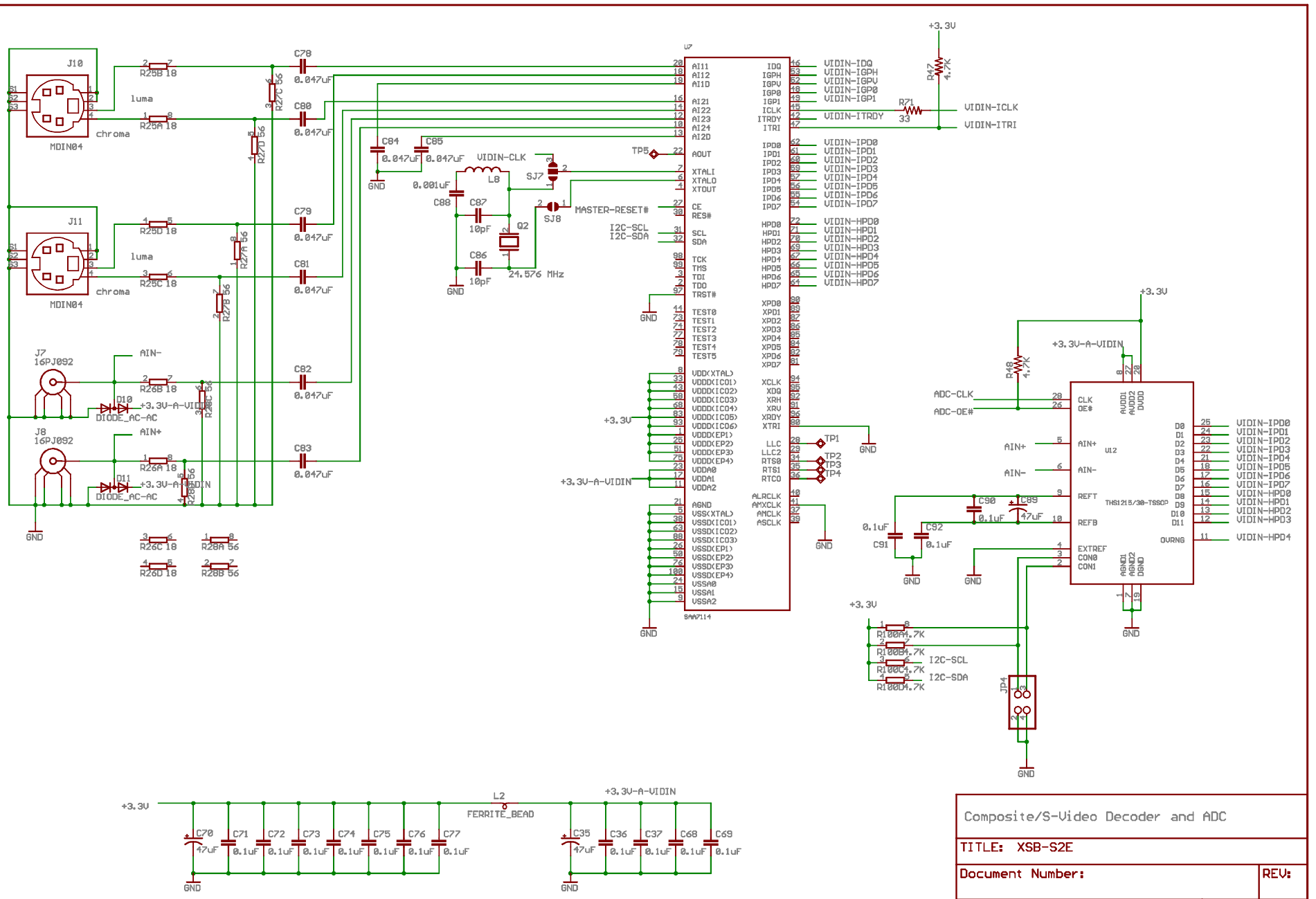
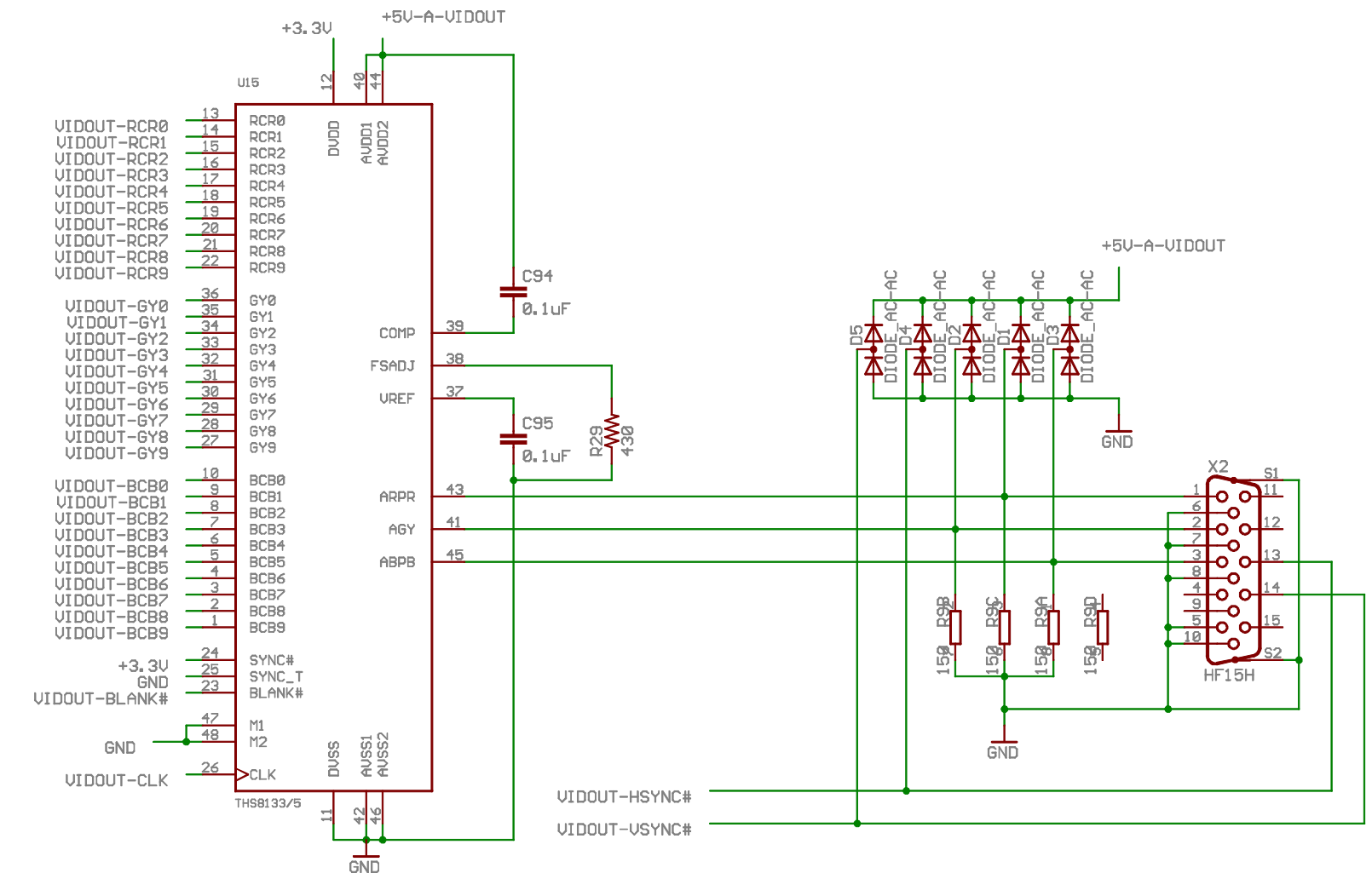

J10
MDIN04
luma
chroma
J11
MDIN04
luma
chroma
J7
16PJ092
AIN-
D10
DIODE_AC-AC
+3.3V-A-VIDIN
J8
16PJ092
AIN+
D11
DIODE_AC-AC
+3.3V-A-VIDIN
R25B 18
R25A 18
R25D 18
R25C 18
R26B 18
R26A 18
R26C 18
R26D 18
R27C 56
R27D 56
R27A 56
R27B 56
R28C 56
R28D 56
R28A 56
R28B 56
C78
C80
C79
C81
C82
C83
0.047uF
GND
U7
SAA7114
C84
C85
0.047uF
0.047uF
VIDIN-CLK
L8
0.001uF
C88
C87
10pF
Q2
C86
10pF
24.576 MHz
SJ7
SJ8
MASTER-RESET#
I2C-SCL
I2C-SDA
TP5
TP1
TP2
TP3
TP4
+3.3V
+3.3V-A-VIDIN
VIDIN-IDQ
VIDIN-IGPH
VIDIN-IGPV
VIDIN-IGP0
VIDIN-IGP1
VIDIN-ITRDY
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
VIDIN-HPD5
VIDIN-HPD6
VIDIN-HPD7
R47 4.7K
R71 33
VIDIN-ICLK
VIDIN-ITRI
+3.3V
+3.3V-A-VIDIN
R48 4.7K
ADC-CLK
ADC-OE#
AIN+
AIN-
C90
C89
47uF
0.1uF
C91
C92
0.1uF
0.1uF
REFT
REFB
EXTREF
CON0
CON1
THS1215/30-TSSOP
U12
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
+3.3V
R100A 4.7K
R100B 4.7K
R100C 4.7K
R100D 4.7K
I2C-SCL
I2C-SDA
JP4
GND
+3.3V
L2
FERRITE_BEAD
+3.3V-A-VIDIN
C70
C71
C72
C73
C74
C75
C76
C77
C35
C36
C37
C68
C69
47uF
0.1uF
GND
Composite/S-Video Decoder and ADC
TITLE: XSB-S2E
Document Number:
REV:
Date: 8/07/2003 10:05:00a
Sheet: 7/16



VGA Video Output

TITLE: XSB-S2E

Document Number:

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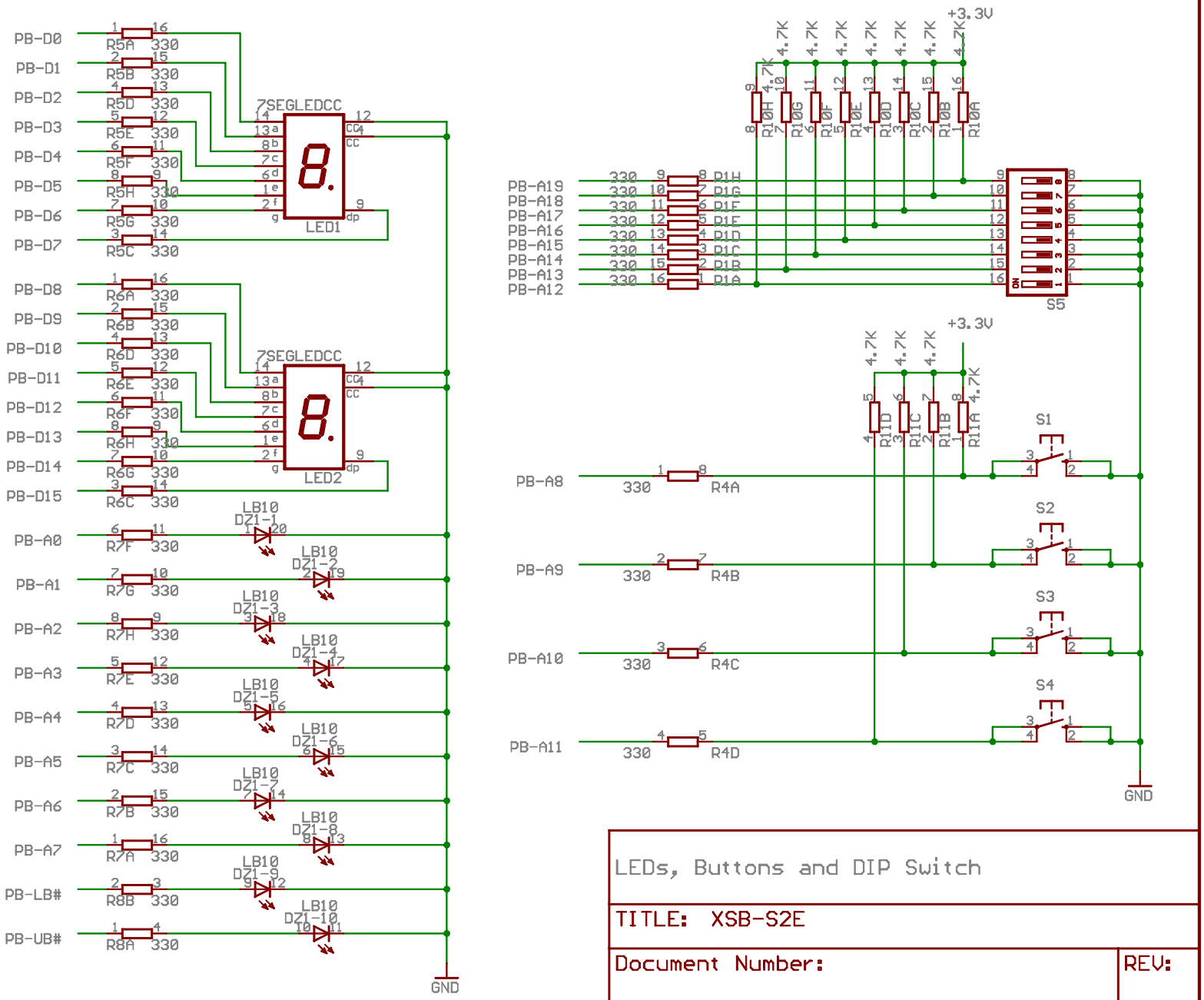
Date: 8/07/2003 10:05:00a

Sheet: 8/16



LEDs, Buttons and DIP Switch

TITLE: XSB-S2E

Document Number:

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Date: 8/07/2003 10:05:00a

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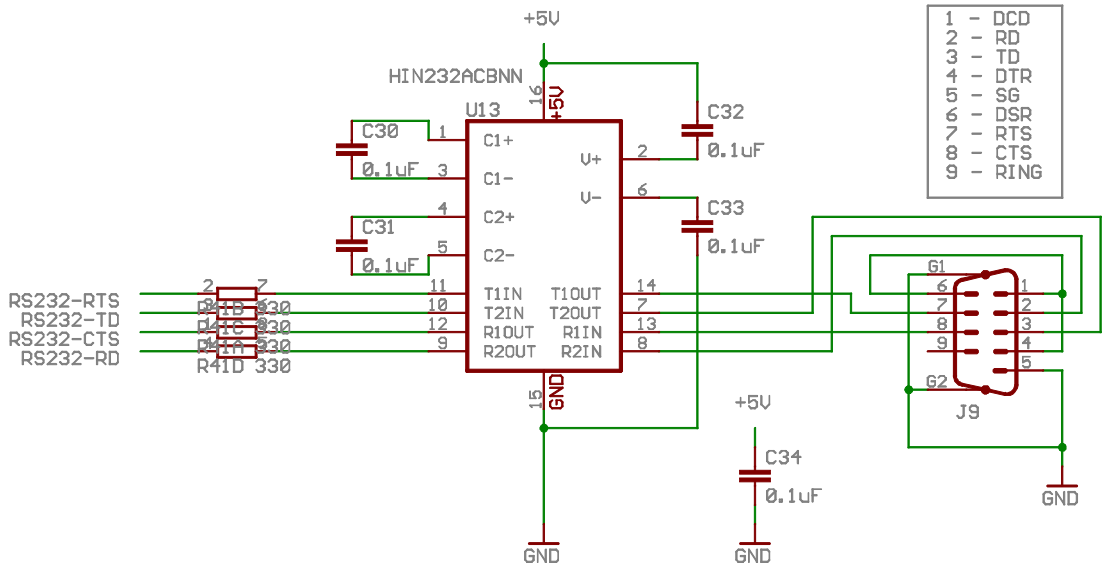

RS-232 Serial Interface		
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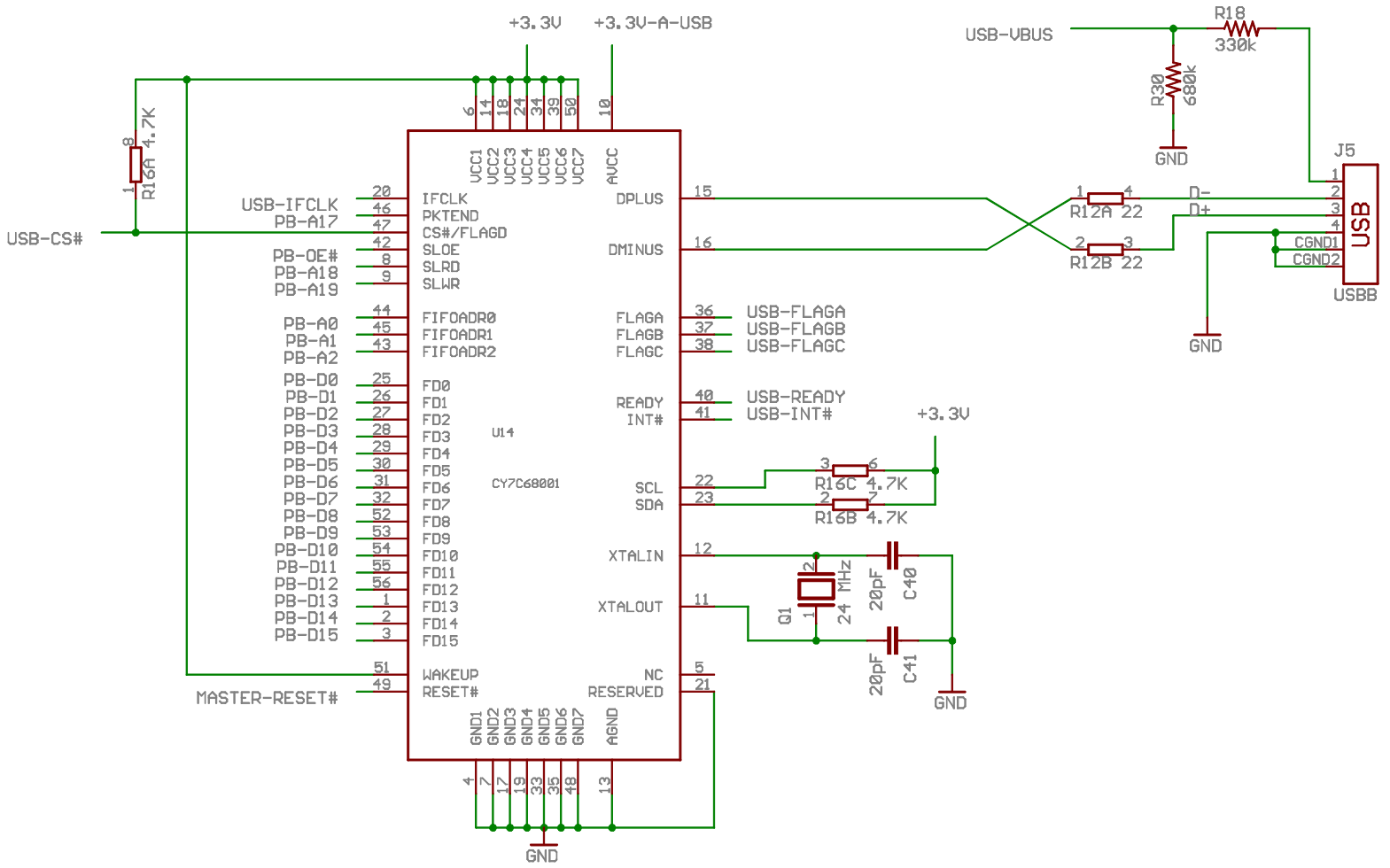
Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 10/16	



USB 2.0 Interface	
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Document Number:	REV:
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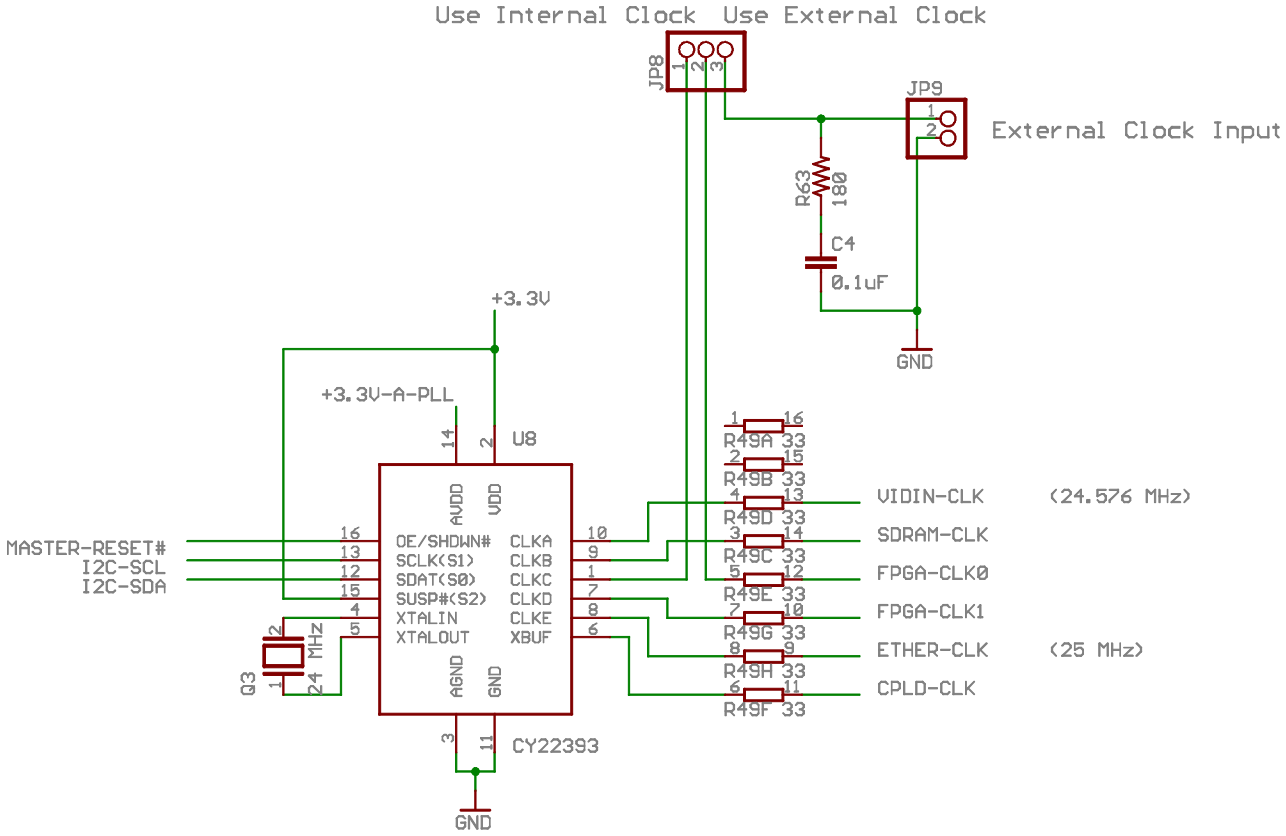

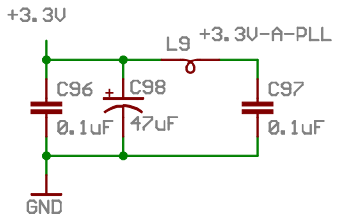

Clock Generator	
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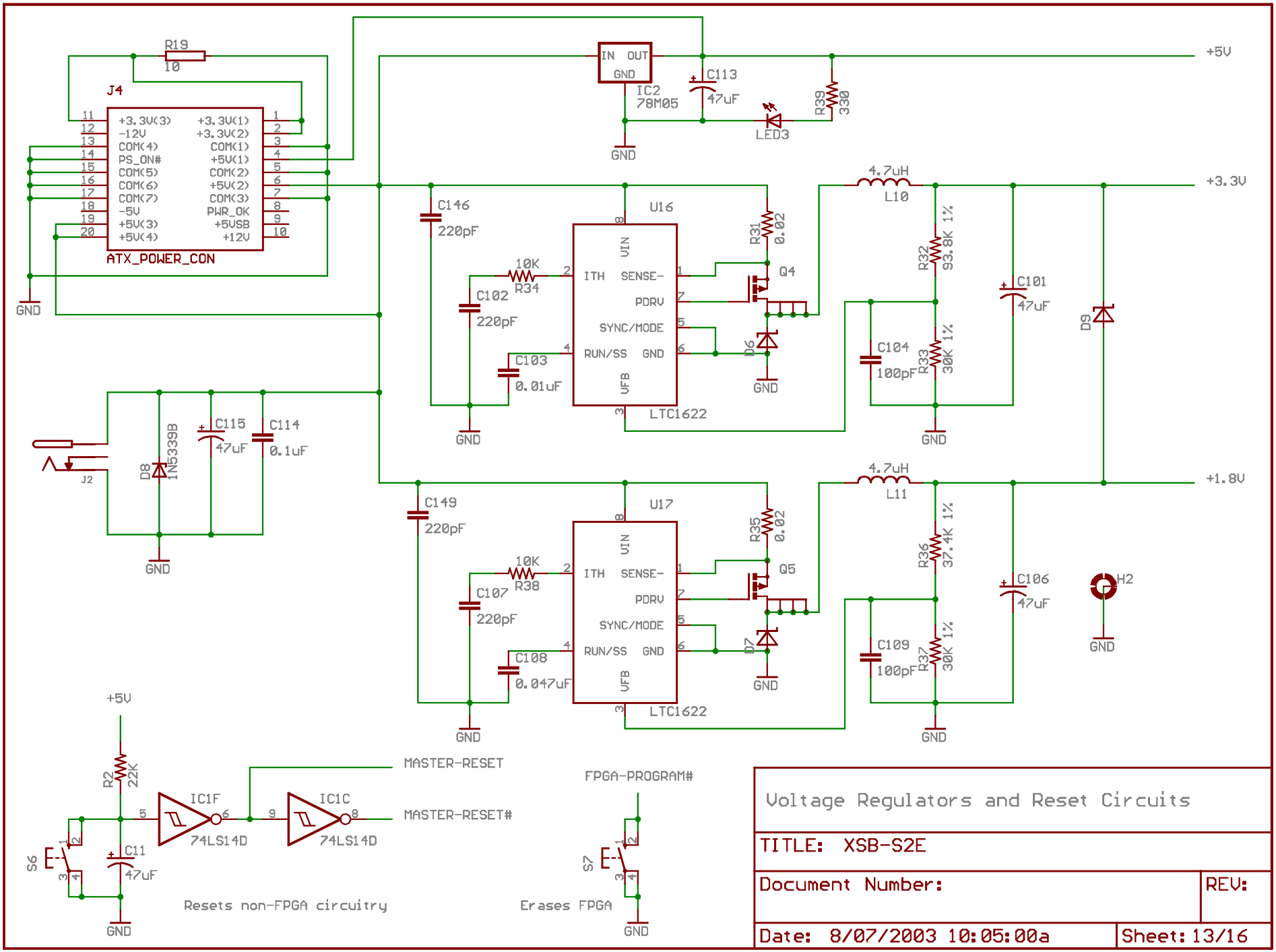
Document Number:	REV:
Date: 8/07/2003 10:05:00a	Sheet: 12/16


R19
10
J4
+3.3V(3)
-12V
COM(4)
PS_ON#
COM(5)
COM(6)
COM(7)
-5V
+5V(3)
+5V(4)
+3.3V(1)
+3.3V(2)
COM(1)
+5V(1)
COM(2)
+5V(2)
COM(3)
PWR_OK
+5VSB
+12V
ATX_POWER_CON
GND
IN OUT
GND
IC2
78M05
C113
47uF
LED3
R39
330
+5V
C146
220pF
U16
VIN
ITH
SENSE-
PDRV
SYNC/MODE
RUN/SS
GND
VFB
LTC1622
10K
R34
C102
220pF
C103
0.01uF
R31
0.02
Q4
D6
4.7uH
L10
R32
93.8K 1%
R33
30K 1%
C104
100pF
C101
47uF
D9
+3.3V
J2
D8
1N5339B
C115
47uF
C114
0.1uF
C149
220pF
U17
LTC1622
10K
R38
C107
220pF
C108
0.047uF
R35
0.02
Q5
D7
4.7uH
L11
R36
37.4K 1%
R37
30K 1%
C109
100pF
C106
47uF
H2
+1.8V
+5V
R2
22K
IC1F
74LS14D
IC1C
74LS14D
MASTER-RESET
MASTER-RESET#
S6
C11
47uF
Resets non-FPGA circuitry
FPGA-PROGRAM#
S7
Erases FPGA
Voltage Regulators and Reset Circuits
TITLE: XSB-S2E
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Date: 8/07/2003 10:05:00a
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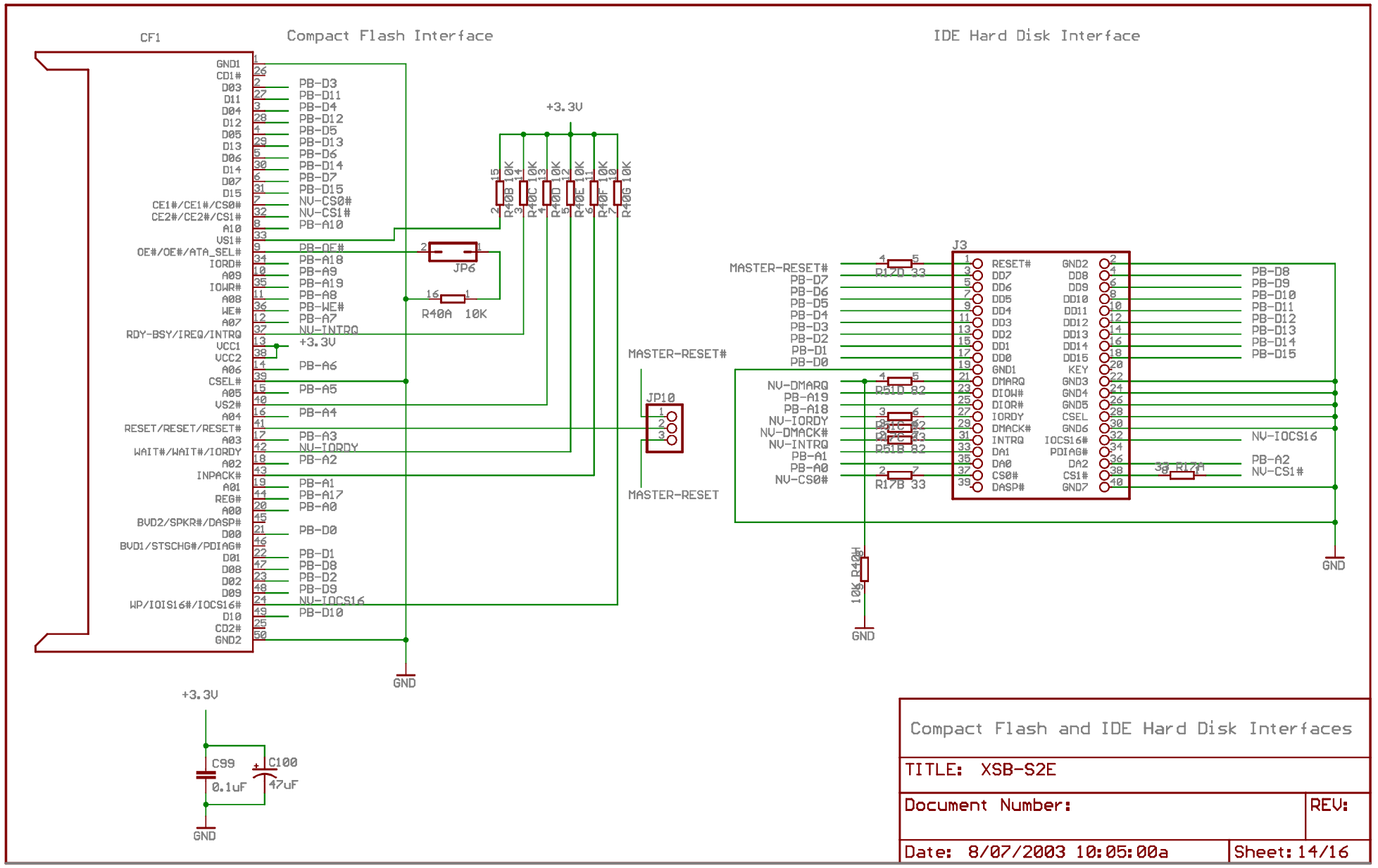
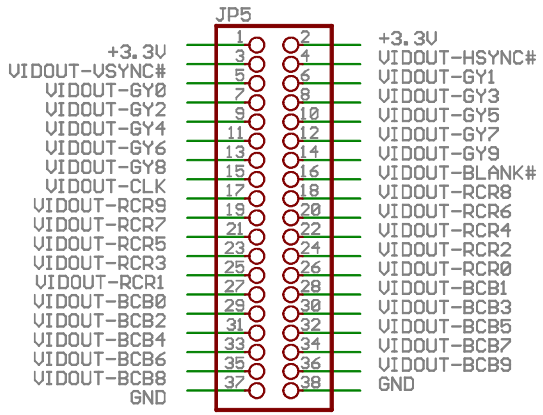
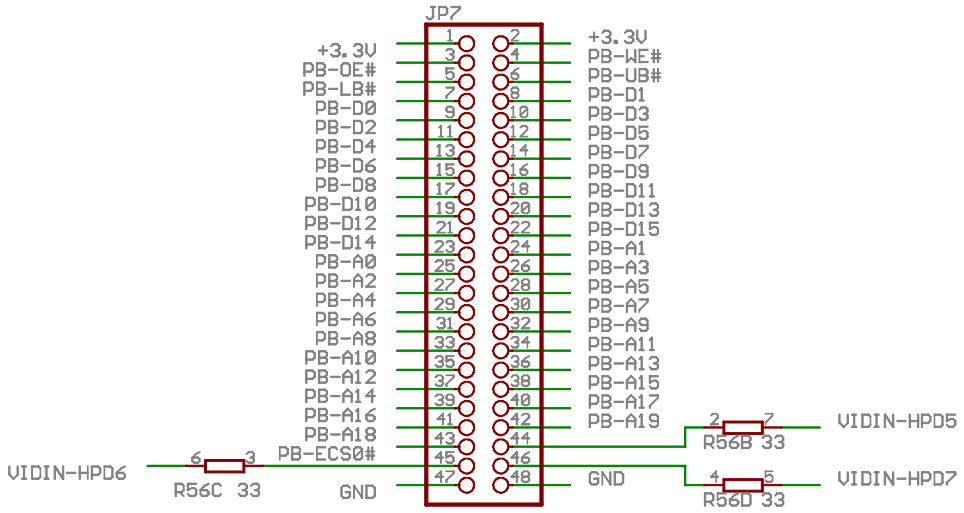


Compact Flash and IDE Hard Disk Interfaces	
TITLE: XSB-S2E	
Document Number:	REV:
Date: 8/07/2003 10:05:00a	Sheet: 14/16

Expansion from Video Output



Expansion from Peripheral Bus



Expansion Connectors		
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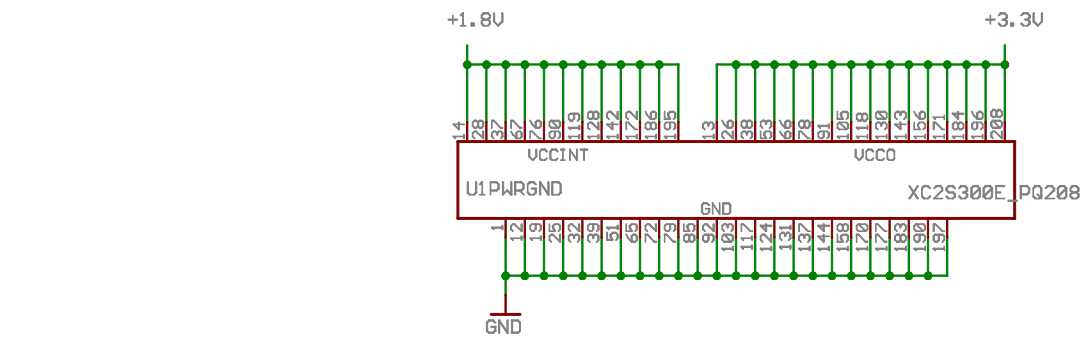
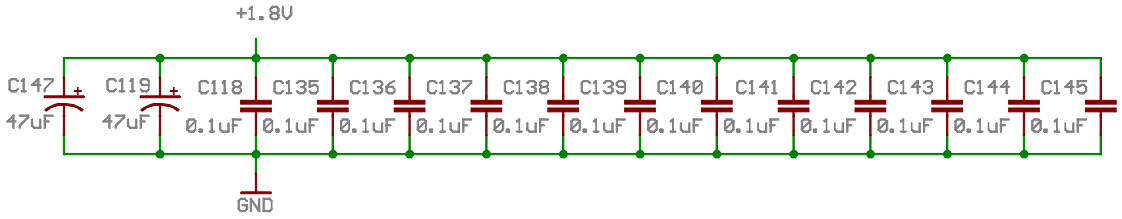
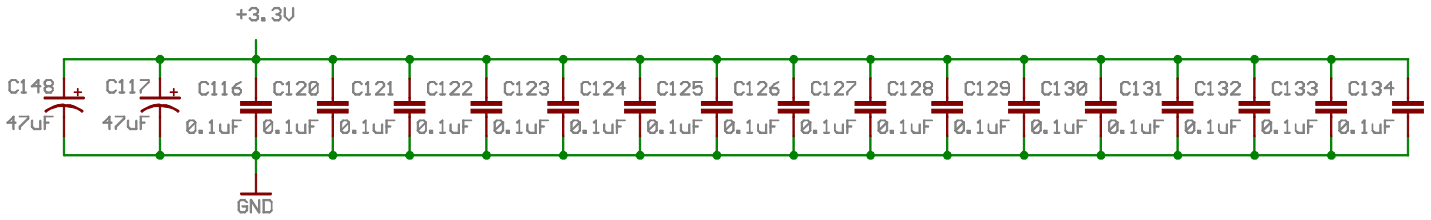
Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 15/16	







FPGA Bypass Capacitors		
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Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 16/16	