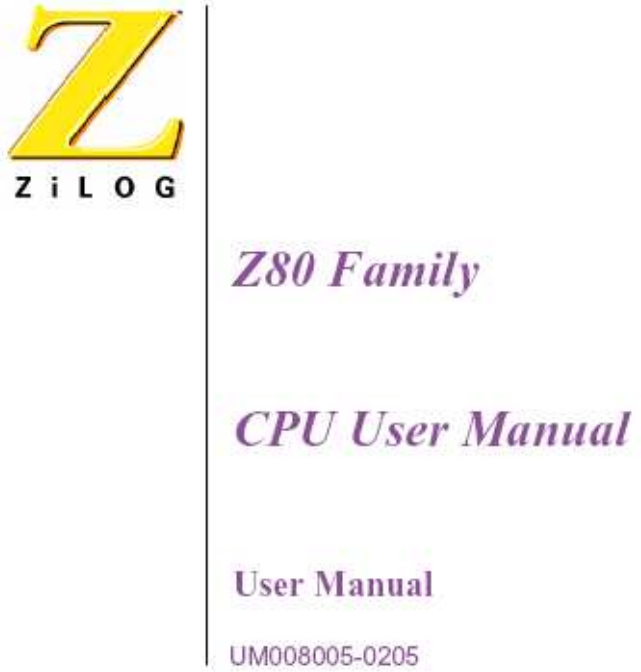
Technika mikroprocesorowa I

Wykład 2

Literatura:

www.zilog.com „Z80 Family, CPU User Manual”



Cykle magistrali w mikroprocesorze Z80

-odczyt kodu rozkazu,

-odczyt-zapis pamięci,

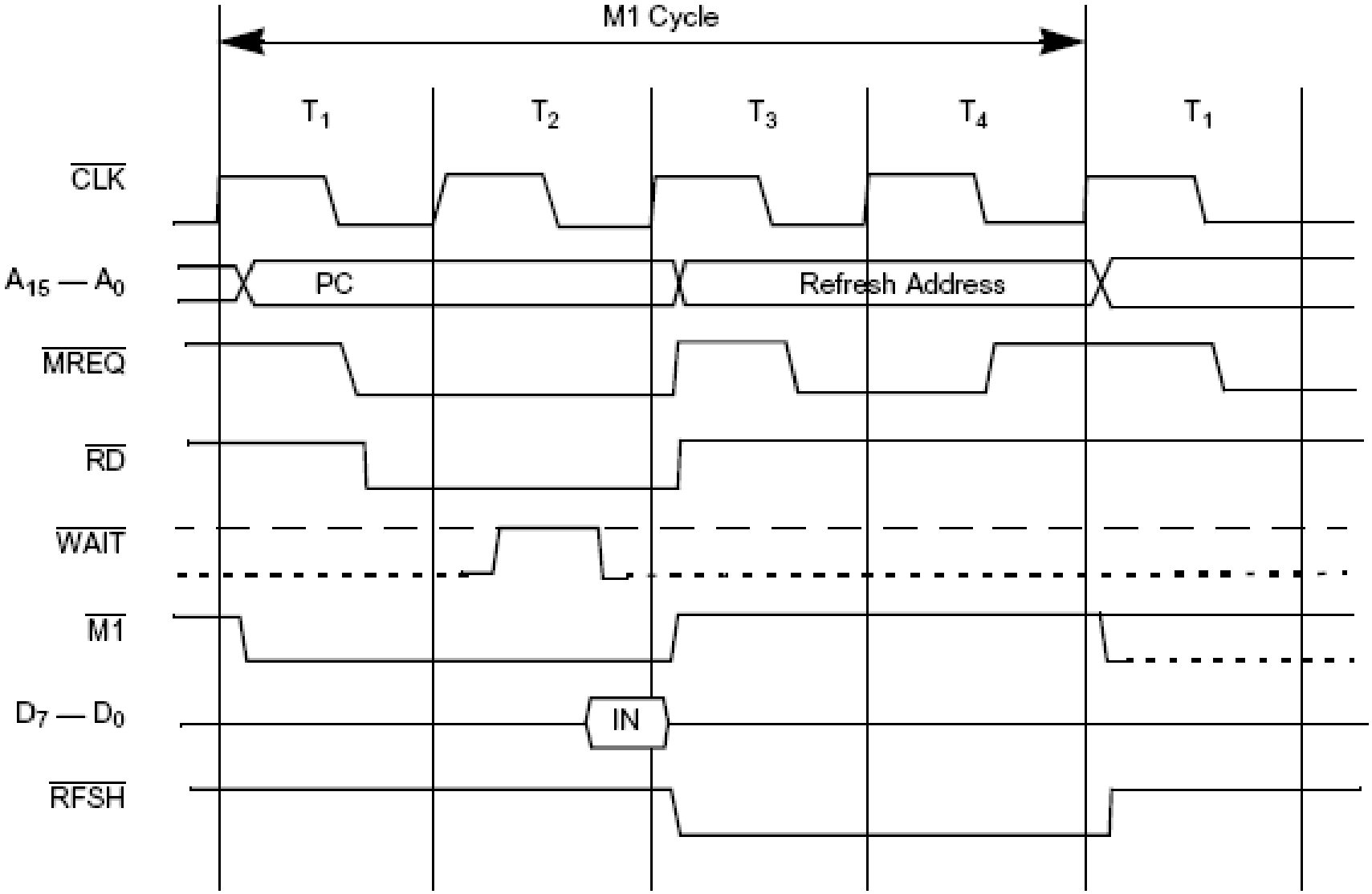
-odczyt-zapis urządzenia we-wy,

-cykl oddania magistrali,

-cykl przyjęcia przerwania maskowalnego,

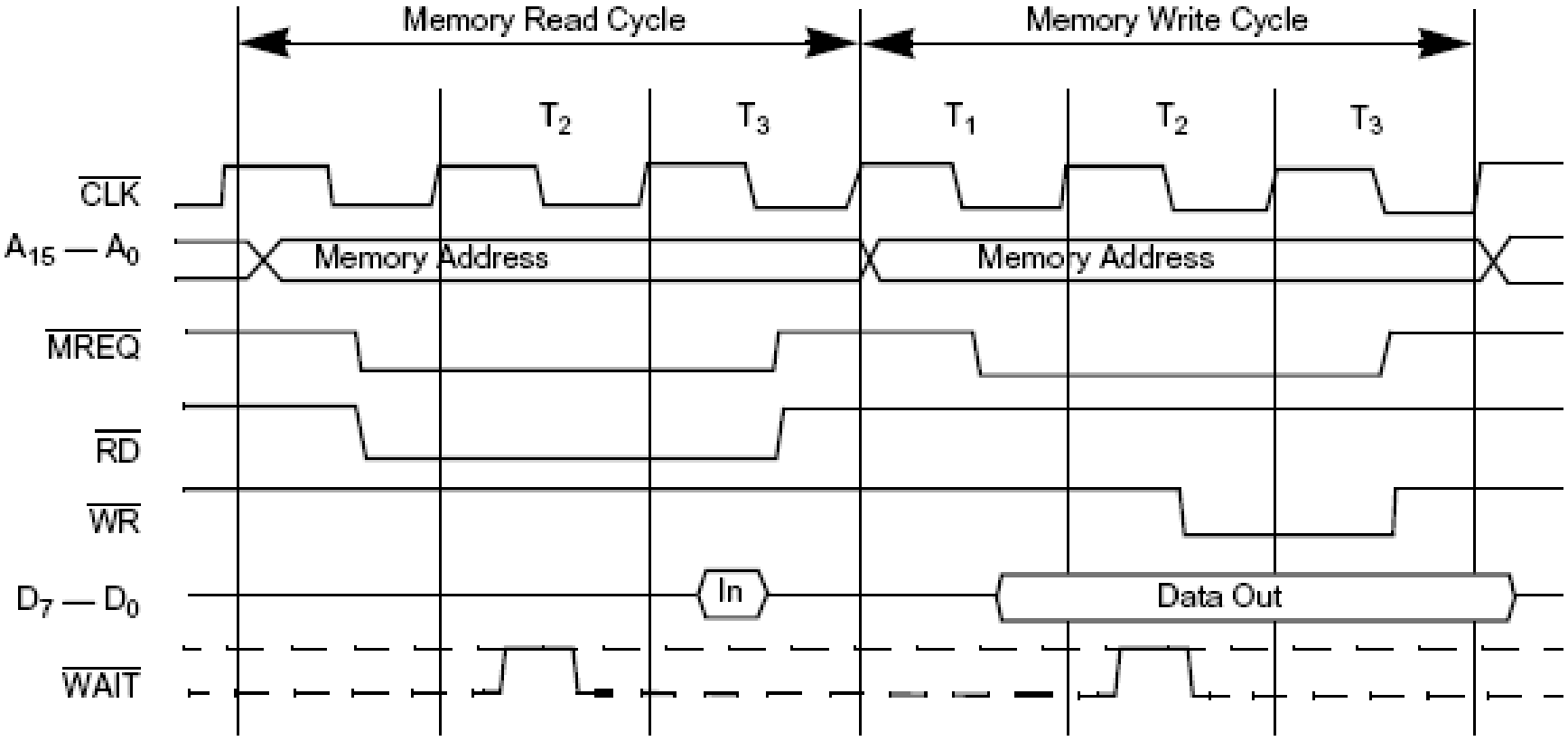
-cykl przyjęcia przerwania niemaskowalnego,

-wyjście z rozkazu HALT.

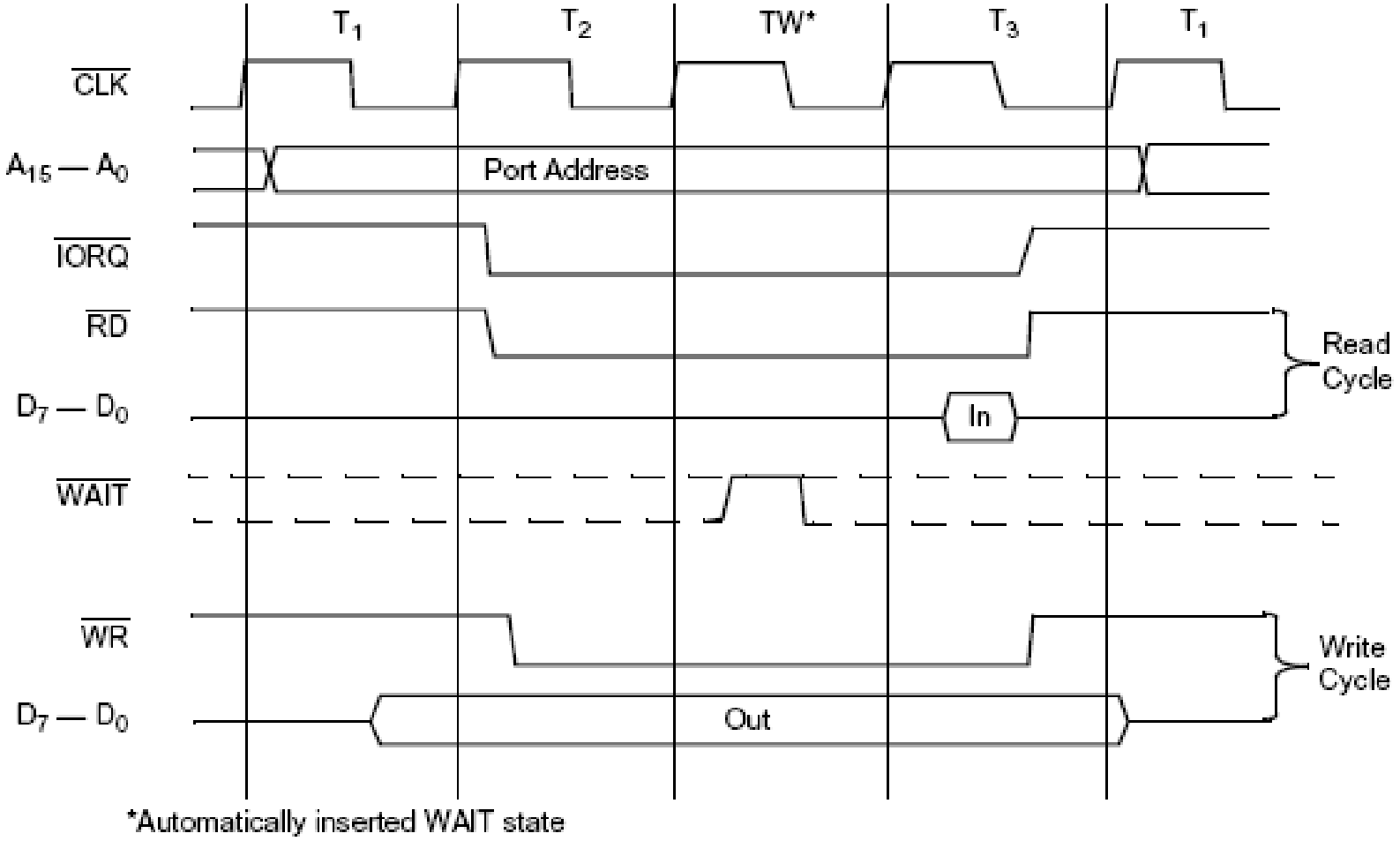


Pobranie kodu rozkazu z pamięci

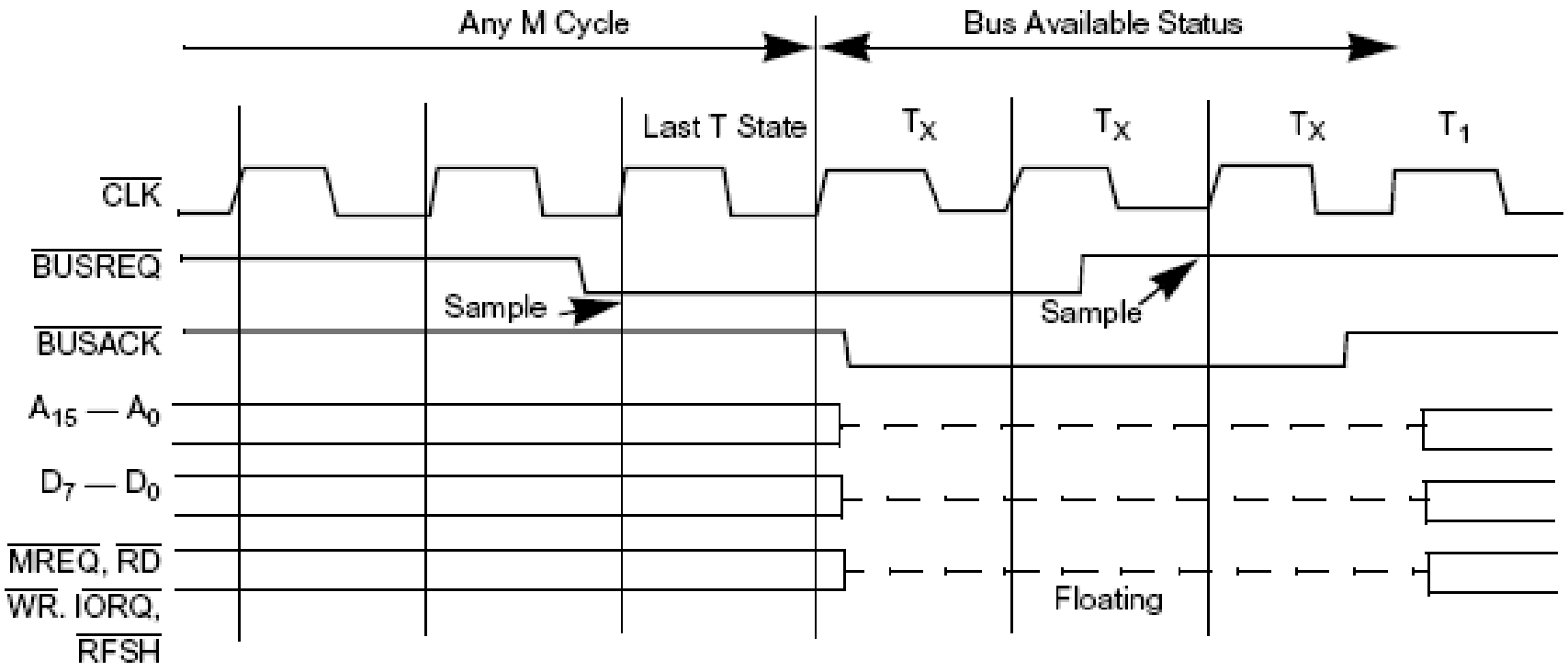
Cykl odczytu i zapisu pamięci



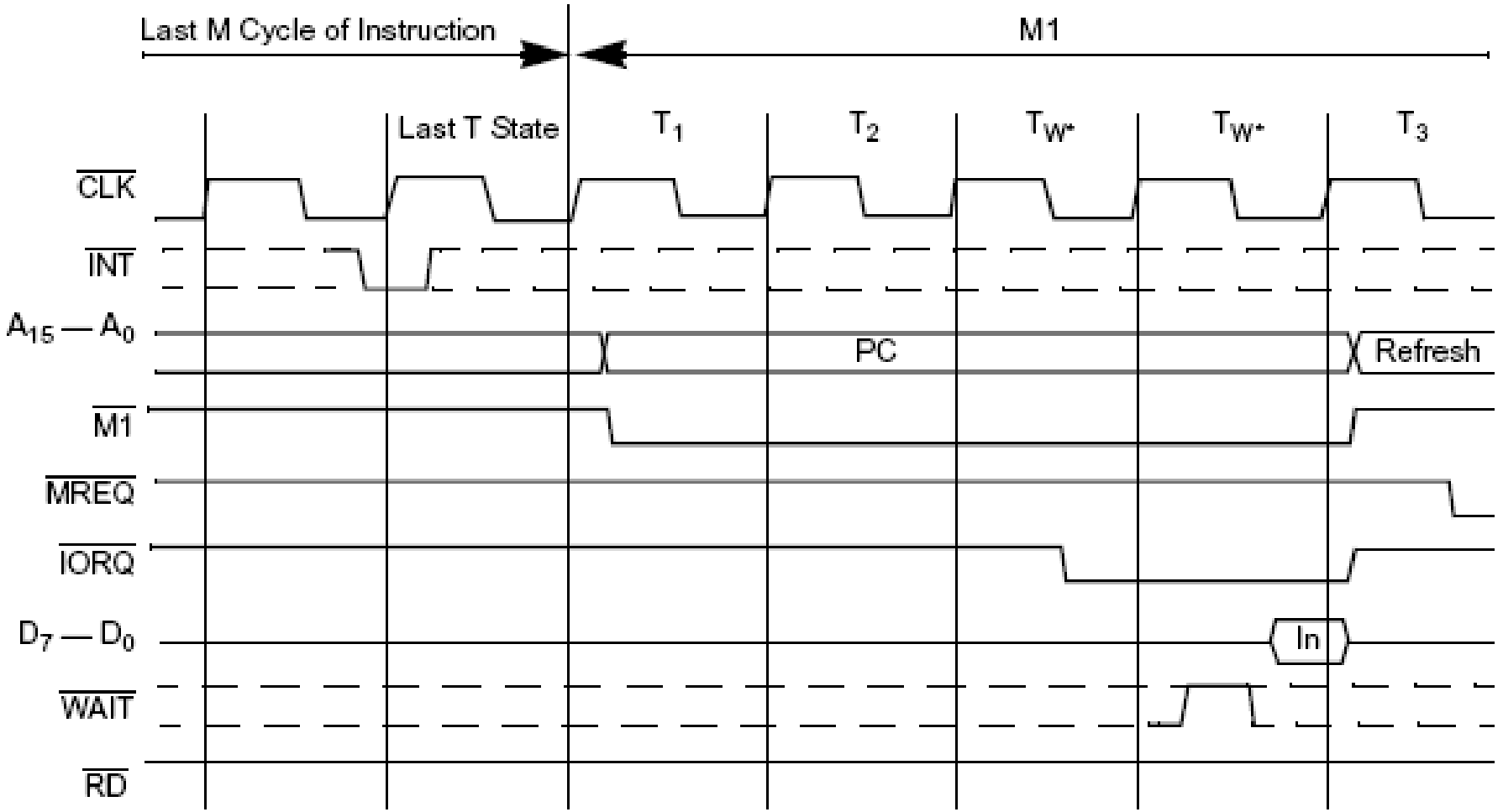
Cykl odczytu i zapisu urządzeń we-wy



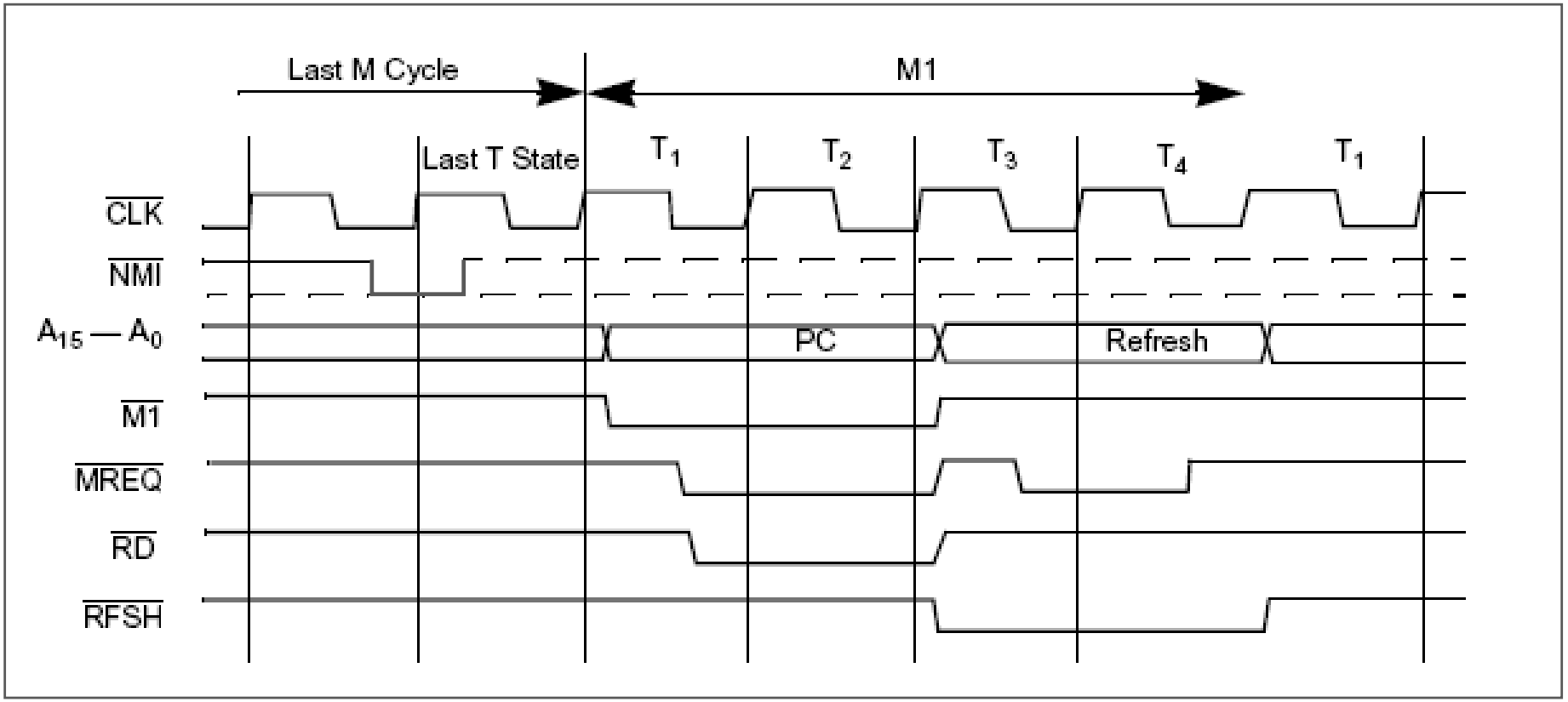
Cykl oddania magistrali



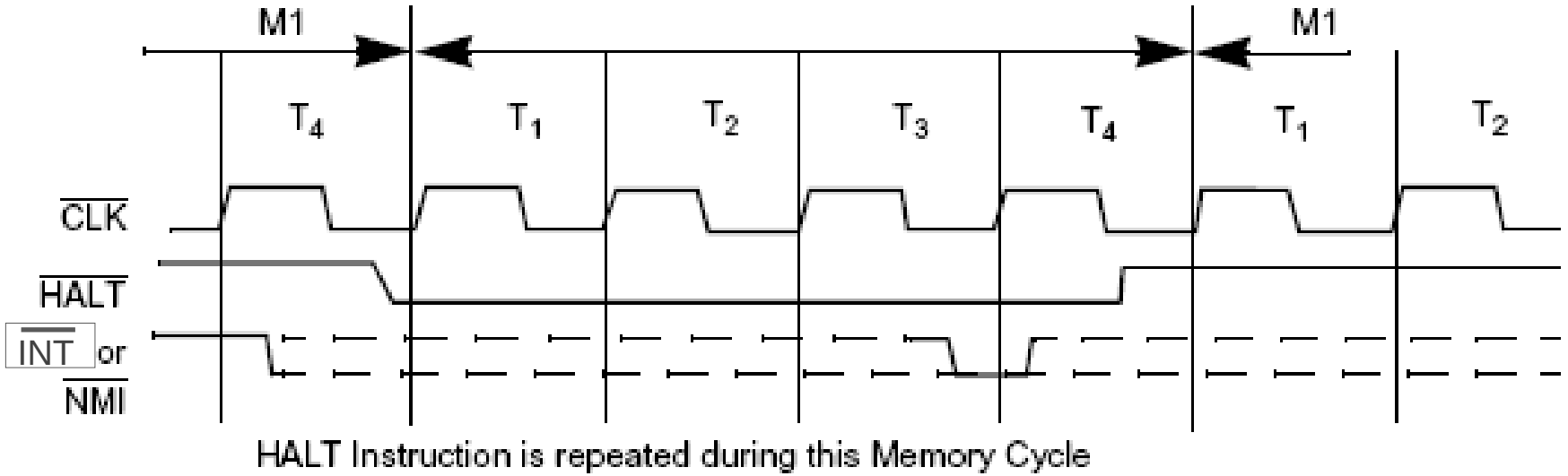
Cykl przyjęcia przerwania maskowalnego



Cykl przyjęcia przerwania niemaskowalnego



Wyjście z rozkazu HALT



System przerwań mikroprocesora Z80

Z80 posiada dwa wejścia zgłaszania przerwań:

NMI- przerwanie niemaskowalne,

INT- przerwanie maskowalne (odmaskowanie rozkazem EI (enable Ibterrupt), zamaskowanie rozkazem DI (Disable Interrupt).

Przerwanie NMI

Przerwanie jest aktywne opadającym zboczem na wejściu **NMI**.

Pojawienie się ujemnego zbocza (przejście z „1” na „0”), powoduje:

-złożenie na stosie adresu powrotu do programu głównego,

-załadowanie do PC adresu 0066h (stały adres obsługi przerwania niemaskowalnego).

Tryby przyjęcia przerwania maskowalnego:

W mikroprocesorze Z80 są 3 tryby przyjmowania przerwania maskowalnego, przełączane rozkazem IMx (Interrupt Mode x-numer modu).

W architekturze wewnętrznej mikroprocesora Z80 istnieją dwa przerzutniki flip-flop odpowiedzialne za aktywację obsługi przerwań maskowalnych. Noszą nazwę odpowiednio: **IFF1 i IFF2**.

IFF1- włącza i wyłącza obsługę przerwań maskowalnych (jest maską przerwań maskowalnych, po RESET- zerowany),

IFF2 -stanowi tymczasowe miejsce przechowywania stanu maski przerwań (stanu przerzutnika- IFF1 jest przepisywany do IFF2), **po RESET IFF1 i IFF2 są zerowane**.

Gdy pojawi się przerwanie **niemaskowalne (wyższy priorytet)**, stan maski przerwań IFF1 jest zapamiętywany w rejestrze bitowym IFF2. Zdekodowanie rozkazu powrotu z przerwania niemaskowalnego NMI (RETN) powoduje odtworzenie stanu IFF1 na podstawie IFF2.

Tryb 0- odpowiada reakcji na przerwania mikroprocesora 8080. W tym trybie urządzenie przerywające, w cyklu akceptacji przerwania, umieszcza na magistrali danych dowolną instrukcję, a mikroprocesor ją wykonuje. Dedykowaną instrukcją jest rozkaz restartu **RST n** (n:0-7). Instrukcja ta powoduje złożenie na stosie adresu powrotu i skok do procedury obsługi zależny od numeru restartu:

n=0 adres 0000h

n=1 adres 0008h

n=2 adres 0010h

n=3 adres 0018h

n=4 adres 0020h

n=5 adres 0028h

n=6 adres 0030h

n=7 adres 0038h

Tryb 1- w tym trybie mikroprocesor reaguje na przerwanie przez wykonanie procedury obsługi od adresu **0038H (po złożeniu na stosie** . Zatem reakcja jest identyczna jak reakcja na przerwanie niemaskowalne, w którym adresem wywoływanym jest adres **0066H**.

Tryb 2- jest najbardziej elastycznym trybem reakcji na przerwanie. W tym trybie programista tworzy tablicę 16-bitowych adresów startowych dla każdej procedury obsługi przerwania. Tablica ta może być umieszczona w dowolnym miejscu w pamięci (decyduje o tym zawartość rejestru I). Gdy przerwanie zostanie przyjęte, urządzenie zgłaszające wystawia na magistrali danych 8-mio bitową, mniej znaczącą, zawsze parzystą część 16-bitowego wskaźnika, w celu pobrania z tablicy adresu startowego obsługi przerwania. W związku z powyższym tryb 2 dopuszcza tylko 128 rozróżnialnych źródeł przerwania.

Tryby adresacji w mikroprocesorze Z80

Mikroprocesor Z80 realizuje następujące tryby adresowania:

-natychmiastowy – argument bezpośrednio za kodem operacji (LD A,0F – załaduj do akumulatora liczbę 0F),

-bezpośredni – dwubajtowy adres argumentu znajduje się w pamięci bezpośrednio za kodem operacji (LD A,(700) – załaduj do akumulatora zawartość komórki pamięci o adresie 0700),

-pośredni erejstrowy – dwubajtowy adres argumentu znajduje się w parze rejestrów BC, DE, HL lub SP (LD A,(BC) –załaduj do akumulatora zawartość komórki pamięci o adresie zawartym w parze rejestrów BC),

-indeksowy– dwubajtowy adres argumentu tworzony jest jako suma zawartości jednego z rejestrów indeksowych IX lub IY i jednobajtowego przesunięcia w kodzie U2 zapisanego za kodem operacji; np. LD A,(IX+8) – załaduj do akumulatora zawartość komórki pamięci o adresie zawartym w rejestrze IX zwiększonym o 8;

-względny– tryb wykorzystywany tylko przez rozkaz skoku względnego JR – zawartość rejestru PC jest modyfikowana przez dodanie jednobajtowego przesunięcia w kodzie U2 umieszczonego w pamięci za kodem operacji skoku;,

-rejestrowy– argument znajduje się w jednym z rejestrów lub w parze rejestrów (w przypadku argumentu 16-bitowego); np. ADD IX,SP – dodaj do zawartości rej. IX wartość rej SP;

-strony zerowej, pojedynczych bitów i implikowany – dotyczą małej liczby rozkazów sterujących (np. RST 8 – wywołanie podprogramu pod adresem 8), logicznych-operacje na pojedynczych bitach (np. RES 0,A – skasowanie bitu 0 w akumulatorze) oraz rozkazów dla których jednoznacznie określone jest położenie argumentu (np. DAA – korekcja dziesiętna akumulatora po operacjach arytmetycznych).

Lista rozkazów mikroprocesora Z80

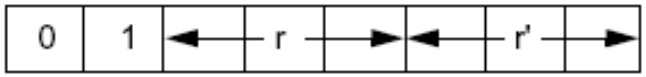
Instrukcje przesyłania danych (8-mio bitowych)

LD r, r'

Operation: r, ← r'

Op Code: LD

Operands: r, r'



Description: The contents of any register r' are loaded to any other register r. r, r' identifies any of the registers A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r, C
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	MHz E.T.
1	4	1.0

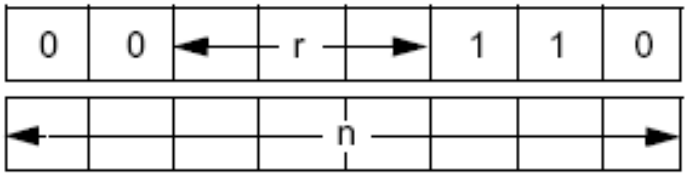
Prześlij zawartość rejestru r’ do rejestru r

LD r,n

Operation: r ← n

Op Code: LD

Operands: r, n



Description: The 8-bit integer n is loaded to any register r, where r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

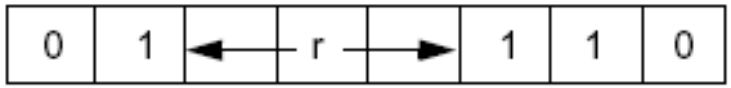
Wpisz do rejestru r liczbę 8-mio bitową n

LD r, (HL)

Operation: r ← (HL)

Op Code: LD

Operands: r, (HL)



Description: The 8-bit contents of memory location (HL) are loaded to register r, where r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

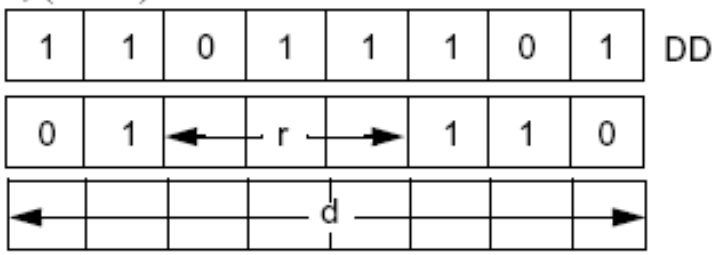
Załaduj do rejestru r zawartość komórki pamięci o adresie zawartym w HL

LD r, (IX+d)

Operation: r ← (IX+d)

Op Code: LD

Operands: r, (IX+d)



Description: The operand (IX+d), (the contents of the Index Register IX summed with a two's complement displacement integer d) is loaded to register r, where r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	2.50

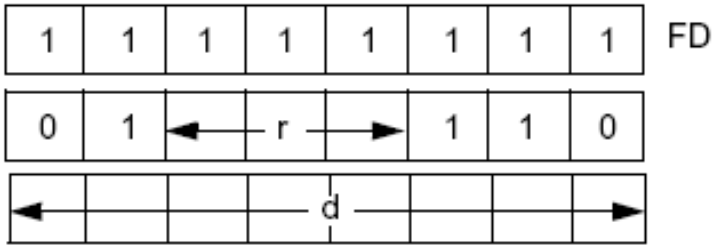
Załaduj do r zawartość komórki o adresie zawartej w IX+ offset d

LD r, (IY+d)

Operation: r ← (IY+D)

Op Code: LD

Operands: r, (IY+d)



Description: The operand (IY+d) (the contents of the Index Register IY summed with a two's complement displacement integer (d) is loaded to register r, where r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	4.75

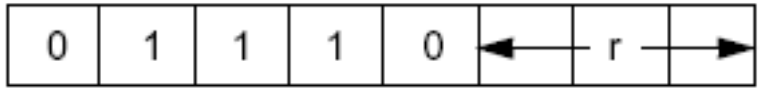
Załaduj do r zawartość komórki o adresie zawartej w IX+ offset d

LD (HL), r

Operation: (HL) ← r

Op Code: LD

Operands: (HL), r



Description: The contents of register r are loaded to the memory location specified by the contents of the HL register pair. The symbol r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

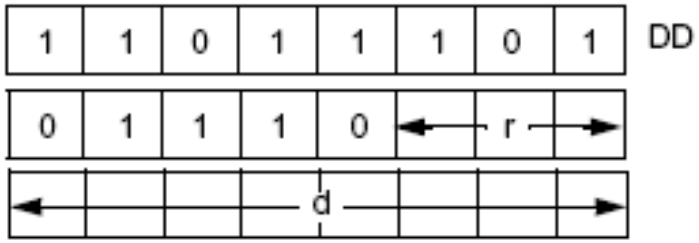
Zapisz zawartość komórki o adresie zawartym w HL do rejestru r

LD (IX+d), r

Operation: (IX+d) ← r

Op Code: LD

Operands: (IX+d), r



Description: The contents of register r are loaded to the memory address specified by the contents of Index Register IX summed with d, a two's complement displacement integer. The symbol r identifies register A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	4.75

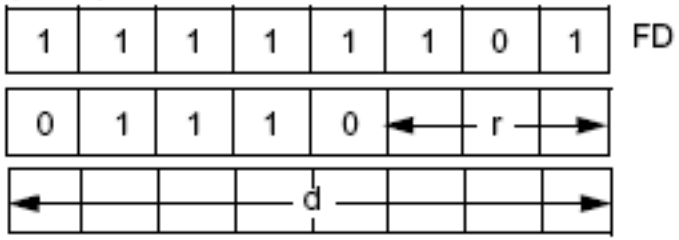
Zapisz zawartość rejestru r do komórki pamięci o adresie zawartym w IX z offsetem d

LD (IY+d), r

Operation: (IY+d) ← r

Op Code: LD

Operands: (IY+d), r



Description: The contents of resister r are loaded to the memory address specified by the sum of the contents of the Index Register IY and d, a two's complement displacement integer. The symbol r is specified according to the following table.

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	4.75

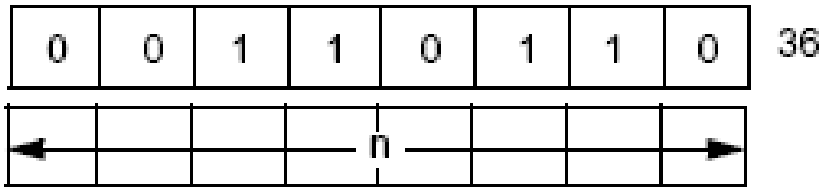
Zapisz zawartość rejestru r do komórki pamięci o adresie zawartym w IY z offsetem d

LD (HL), n

Operation: (HL) ← n

Op Code: LD

Operands: (HL), n



Description: Integer n is loaded to the memory address specified by the contents of the HL register pair.

M Cycles	T States	4 MHz E.T.
3	10 (4, 3, 3)	2.50

Condition Bits Affected: None

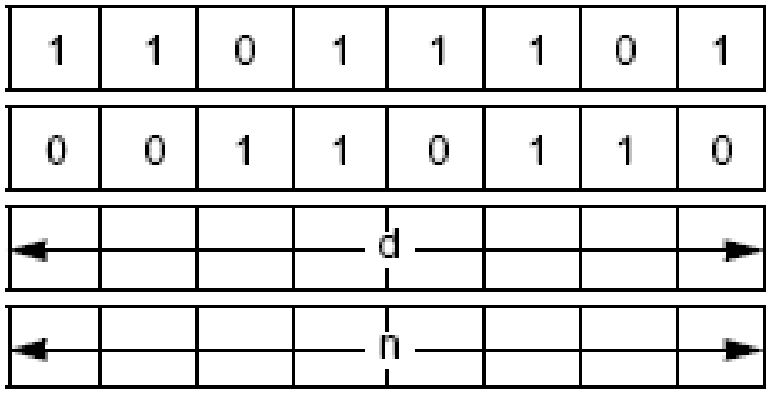
Zapisz do komórki o adresie zawartym w HL liczbę 8-mio bitową n

LD (IX+d), n

Operation: (IX+d) ← n

Op Code: LD

Operands: (IX+d), n



Description: The n operand is loaded to the memory address specified by the sum of the Index Register IX and the two's complement displacement operand d.

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3,5,3)	4.75

Condition Bits Affected: None

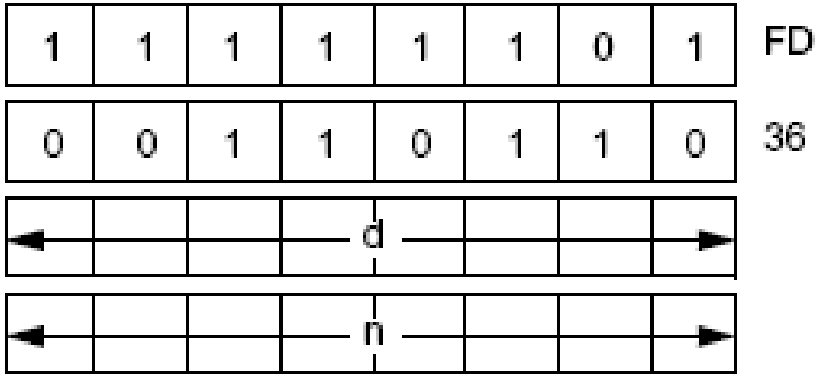
Zapisz do komórki o adresie zawartym w IX+ offset d, liczbę 8-mio bitową n

LD (IY+d), n

Operation: (IY+d) ← n

Op Code: LD

Operands: (IY+d), n



Description: Integer n is loaded to the memory location specified by the contents of the Index Register summed with the two's complement displacement integer d.

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	2.50

Condition Bits Affected: None

Zapisz do komórki o adresie zawartym w IY+ offset d, liczbę 8-mio bitową n

LD A, (BC)

Operation: A ← (BC)

Op Code: LD

Operands: A, (BC)

0	0	0	0	1	0	1	0	0A

Description: The contents of the memory location specified by the contents of the BC register pair are loaded to the Accumulator.

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

Załaduj do akumulatora A zawartość komórki pamięci o adresie zawartym w parze rejestrów BC

LD A, (DE)

Operation: A ← (DE)

Op Code: LD

Operands: A, (DE)

0	0	0	1	1	0	1	0	1A

Description: The contents of the memory location specified by the register pair DE are loaded to the Accumulator.

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

Condition Bits Affected: None

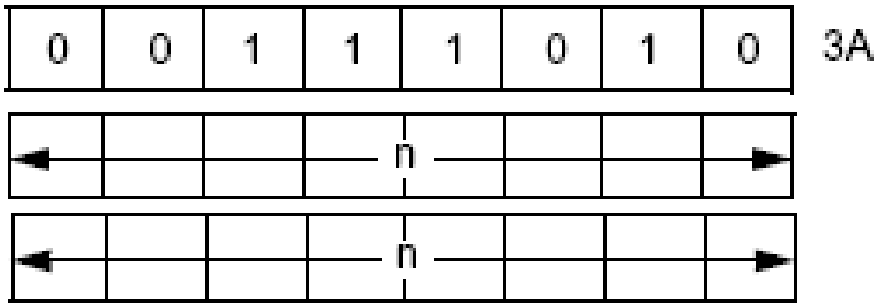
Załaduj do akumulatora A zawartość komórki pamięci o adresie zawartym w parze rejestrów DE

LD A, (nn)

Operation: A ← (nn)

Op Code: LD

Operands: A, (nn)



Description: The contents of the memory location specified by the operands nn are loaded to the Accumulator. The first n operand after the Op Code is the low order byte of a 2-byte memory address.

M Cycles	T States	4 MHz E.T.
4	13 (4, 3, 3, 3)	3.25

Załaduj do akumulatora A zawartość komórki pamięci o adresie nn

LD (BC), A

Operation: (BC) ← A

Op Code: LD

Operands: (BC), A

0	0	0	0	0	0	1	0	02

Description: The contents of the Accumulator are loaded to the memory location specified by the contents of the register pair BC.

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

Załaduj zawartość akumulatora do komórki pamięci o adresie zawartym w parze rejestrów BC

LD (DE), A

Operation: (DE) ← A

Op Code: LD

Operands: (DE), A

0	0	0	1	0	0	1	0	12

Description: The contents of the Accumulator are loaded to the memory location specified by the contents of the DE register pair.

M cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

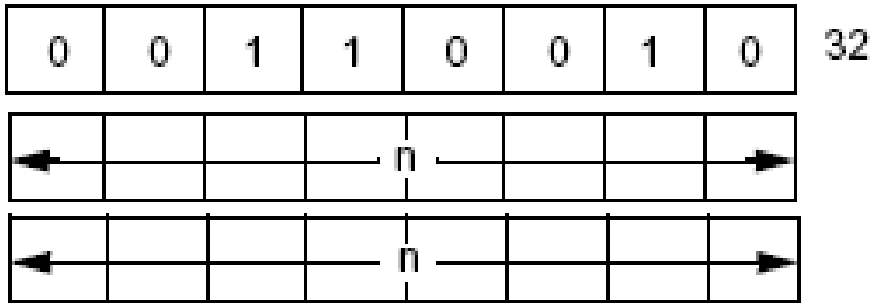
Załaduj zawartość akumulatora do komórki pamięci o adresie zawartym w parze rejestrów DE

LD (nn), A

Operation: (nn) ← A

Op Code: LD

Operands: (nn), A



Description: The contents of the Accumulator are loaded to the memory address specified by the operand nn. The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
4	13 (4, 3, 3, 3)	3.25

Załaduj zawartość akumulatora A do komórki pamięci o adresie nn

LD A, I

Operation: $A \leftarrow I$

Op Code: LD

Operands: A, I

1	1	1	0	1	1	0	1	ED
0	1	0	1	0	1	1	1	57

Description: The contents of the Interrupt Vector Register I are loaded to the Accumulator.

M Cycles	T States	MHz E.T.
2	9 (4, 5)	2.25

Przepisz zawartość rejestru adresu tablicy przerwań do rejestru A

LD A, R

Operation: A, ← R

Op Code: LD

Operands: A, R

1	1	1	0	1	1	0	1	ED
0	1	0	1	1	1	1	1	5F

Description: The contents of Memory Refresh Register R are loaded to the Accumulator.

M Cycles	T States	MHz E.T.
2	9 (4, 5)	2.25

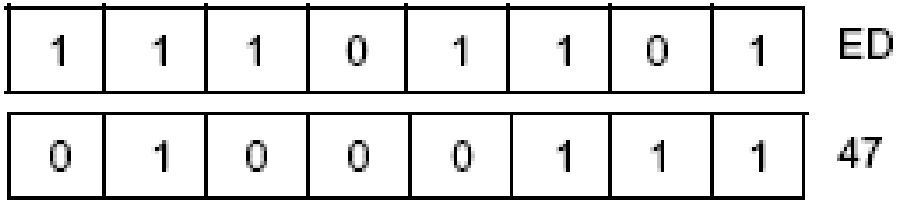
Przepisz zawartość rejestru odświeżania do rejestru A

LD I,A

Operation: I ← A

Op Code: LD

Operands: I, A



Description: The contents of the Accumulator are loaded to the Interrupt Control Vector Register, I.

M Cycles	T States	MHz E.T.
2	9 (4, 5)	2.25

Zapisz zawartość akumulatora do rejestru adresu tablicy przerwań

LD R, A

Operation: R ← A

Op Code: LD

Operands: R, A

1	1	1	0	1	1	0	1	ED
0	1	0	0	1	1	1	1	4F

Description: The contents of the Accumulator are loaded to the Memory Refresh register R.

M Cycles	T States	MHz E.T.
2	9 (4, 5)	2.25

Zapisz zawartość akumulatora do rejestru odświeżania

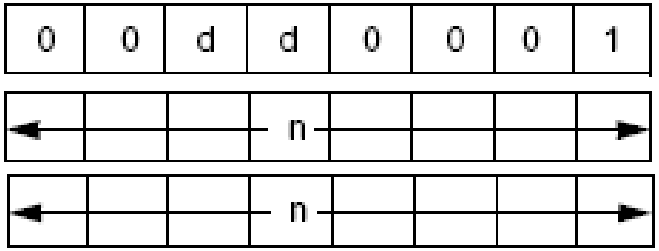
Instrukcje przesyłania danych (16-to bitowych)

LD dd, nn

Operation: dd ← nn

Op Code: LD

Operands: dd, nn



Description: The 2-byte integer nn is loaded to the dd register pair, where dd defines the BC, DE, HL, or SP register pairs, assembled as follows in the object code:

Pair	dd
BC	00
DE	01
HL	10
SP	11

The first n operand after the Op Code is the low order byte.

M Cycles	T States	4 MHz E.T.
2	10 (4, 3, 3)	2.50

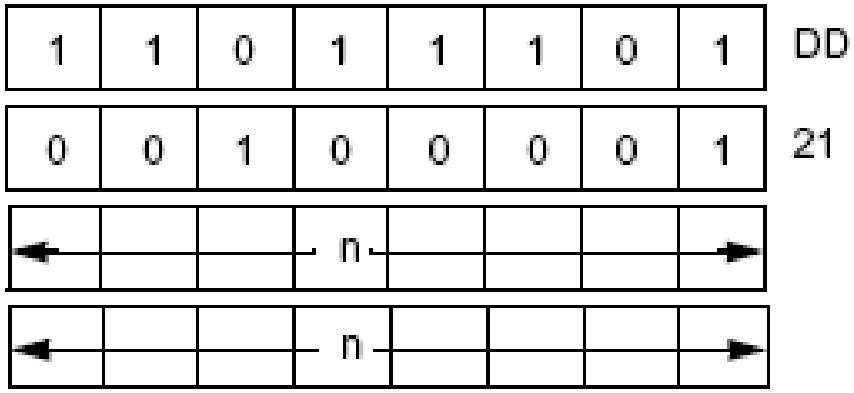
Zapisz do pary rejestrów dd daną 16-to bitową nn

LD IX, nn

Operation: Ix ← nn

Op Code: LD

Operands: IX, nn



Description: Integer nn is loaded to the Index Register IX. The first n operand after the Op Code is the low order byte.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

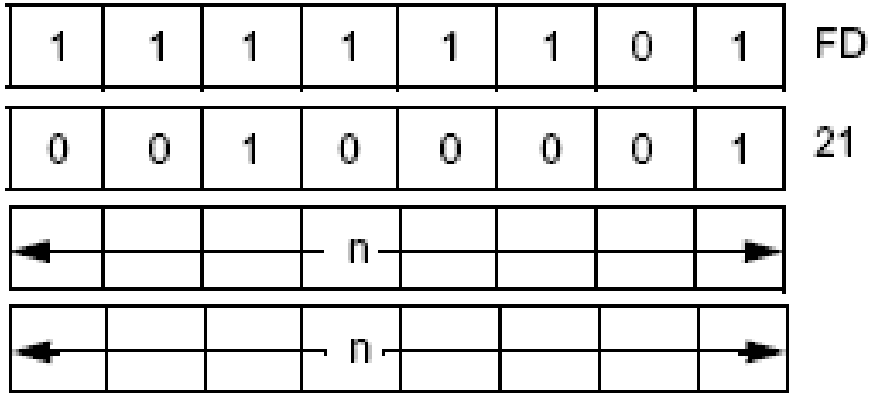
Zapisz do rejestru indeksowego IX liczbę 16-to bitową nn

LD IY, nn

Operation: IY ← nn

Op Code: LD

Operands: IY, nn



Description: Integer nn is loaded to the Index Register IY. The first n operand after the Op Code is the low order byte.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

Condition Bits Affected: None

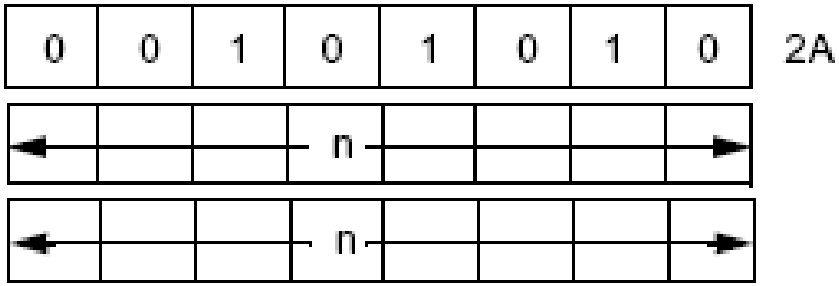
Zapisz do rejestru indeksowego IY liczbę 16-to bitową nn

LD HL, (nn)

Operation: H ← (nn+1), L ← (nn)

Op Code: LD

Operands: HL, (nn)



Description: The contents of memory address (nn) are loaded to the low order portion of register pair HL (register L), and the contents of the next highest memory address (nn+1) are loaded to the high order portion of HL (register H). The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
5	16 (4, 3, 3, 3, 3)	4.00

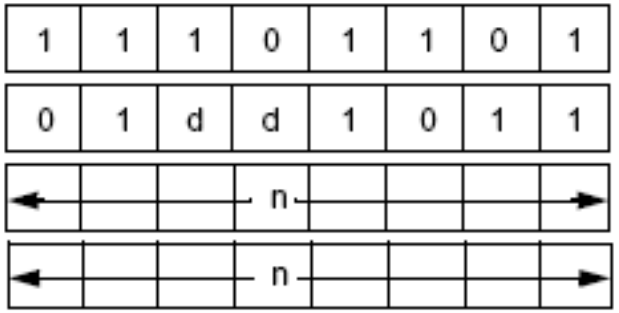
Załadowanie zawartość dwóch kolejnych komórek pamięci spod adresu nn do pary rejestrów HL

LD dd, (nn)

Operation: ddh ← (nn+1) ddl ← (nn)

Op Code: LD

Operands: dd, (nn)



Description: The contents of address (nn) are loaded to the low order portion of register pair dd, and the contents of the next highest memory address (nn+1) are loaded to the high order portion of dd. Register pair dd defines BC, DE, HL, or SP register pairs, assembled as follows in the object code:

Pair	dd
BC	00
DE	01
HL	10
SP	11

The first n operand after the Op Code is the low order byte of (nn).

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

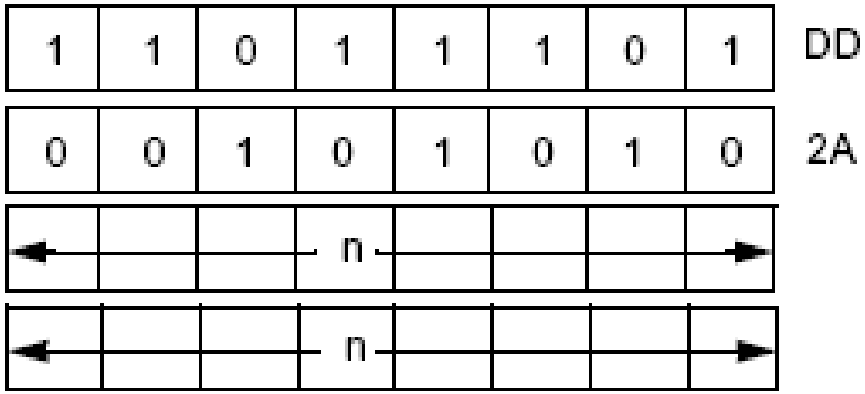
Załadowanie do pary rejestrów dd zawartości komórek pamięci spod adresu nn

LD IX, (nn)

Operation: IXh ← (nn+1), IXl ← (nn)

Op Code: LD

Operands: IX, (nn)



Description: The contents of the address (nn) are loaded to the low order portion of Index Register IX, and the contents of the next highest memory address (nn+1) are loaded to the high order portion of IX. The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

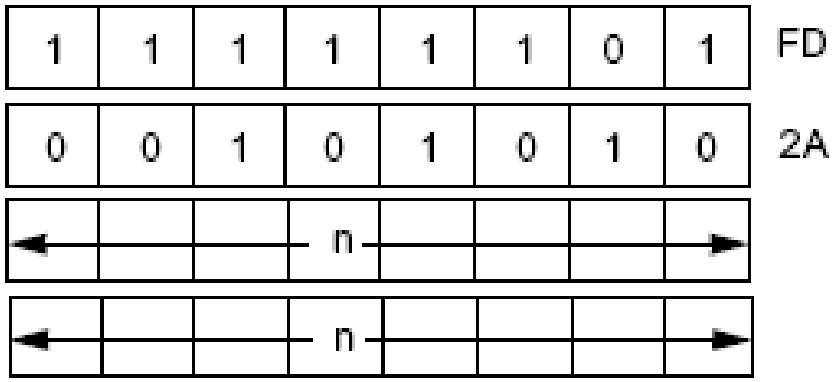
Załadowanie do IX zawartości komórek pamięci spod adresu nn

LD IY, (nn)

Operation: IYh ← (nn+1), IYI ← nn)

Op Code: LD

Operands: IY, (nn)



Description: The contents of address (nn) are loaded to the low order portion of Index Register IY, and the contents of the next highest memory address (nn+1) are loaded to the high order portion of IY. The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

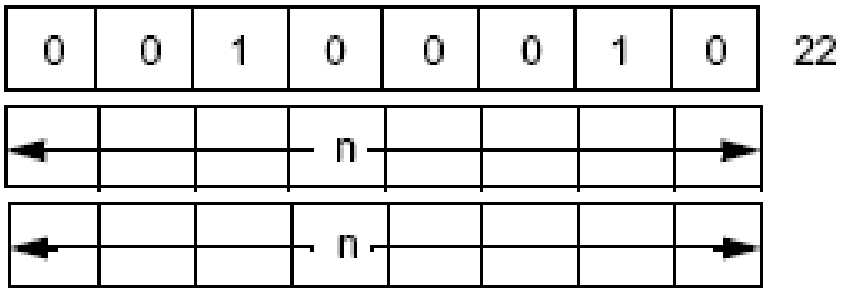
Załadowanie do IY zawartości komórek pamięci spod adresu nn

LD (nn), HL

Operation: (nn+1) ← H, (nn) ← L

Op Code: LD

Operands: (nn), HL



Description: The contents of the low order portion of register pair HL (register L) are loaded to memory address (nn), and the contents of the high order portion of HL (register H) are loaded to the next highest memory address (nn+1). The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
5	16 (4, 3, 3, 3, 3)	4.00

Condition Bits Affected: None

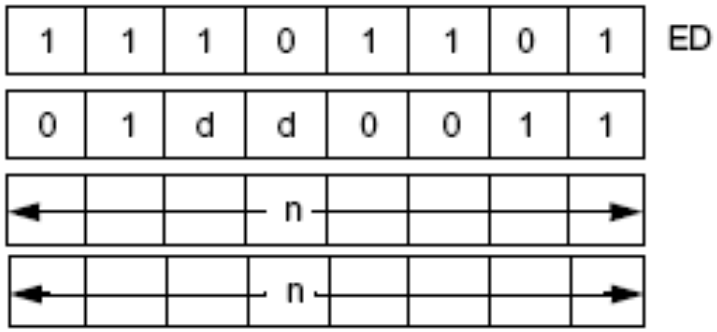
Załaduj do komórek pod adresem nn zawartość rejestru HL

LD (nn), dd

Operation: (nn+1) ← ddh, (nn) ← ddl

Op Code: LD

Operands: (nn), dd



Description: The low order byte of register pair dd is loaded to memory address (nn); the upper byte is loaded to memory address (nn+1). Register pair dd defines either BC, DE, HL, or SP, assembled as follows in the object code:

Pair	dd
BC	00
DE	01
HL	10
SP	11

The first n operand after the Op Code is the low order byte of a two byte memory address.

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

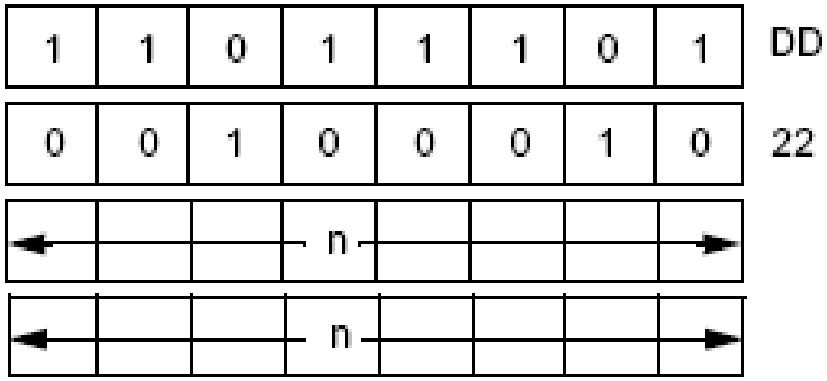
Załaduj zawartość pary rejestrów dd do komórek pamięci od adresu nn

LD (nn), IX

Operation: (nn+1) ← IXh, (nn) ← IXI

Op Code: LD

Operands: (nn), IX



Description: The low order byte in Index Register IX is loaded to memory address (nn); the upper order byte is loaded to the next highest address (nn+1). The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

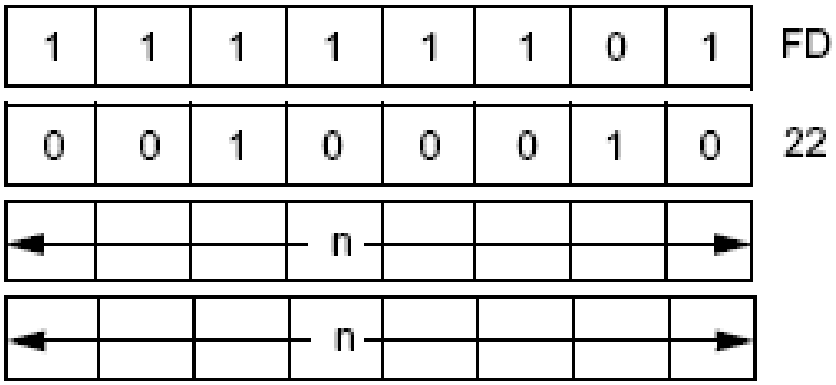
Załaduj zawartość rejestru IX do komórek pamięci od adresu nn

LD (nn), IY

Operation: (nn+1) ← IYh, (nn) ← IYl

Op Code: LD

Operands: (nn), IY



Description: The low order byte in Index Register IY is loaded to memory address (nn); the upper order byte is loaded to memory location (nn+1). The first n operand after the Op Code is the low order byte of nn.

M Cycles	T States	4 MHz E.T.
6	20 (4, 4, 3, 3, 3, 3)	5.00

Condition Bits Affected: None

Załaduj zawartość rejestru IY do komórek pamięci od adresu nn

LD SP, HL

Operation: SP ← HL

Op Code: LD

Operands: SP, HL

1	1	1	r	1	0	0	1	F9

Description: The contents of the register pair HL are loaded to the Stack Pointer (SP).

M Cycles	T States	4 MHz E.T.
1	6	1.5

Zapisz zawartość rejestru HL do rejestru SP

LD SP, IX

Operation: SP ← - IX

Op Code: LD

Operands: SP, 1X

1	1	0	1	1	1	0	1	DD
1	1	1	1	1	0	0	1	F9

Description: The 2-byte contents of Index Register IX are loaded to the Stack Pointer (SP).

M Cycles	T States	4 MHz E.T.
2	10 (4, 6)	2.50

Przepisz zawartość rejestru IX do rejestru SP

LD SP, IY

Operation: SP ← IY

Op Code: LD

Operands: SP, IY

1	1	1	1	1	1	0	1	FD
1	1	1	1	1	0	0	1	F9

Description: The 2-byte contents of Index Register IY are loaded to the Stack Pointer SP.

M Cycles	T States	4 MHz E.T.
2	10 (4, 6)	2.50

Condition Bits Affected: None

Przepisz zawartość rejestru IY do rejestru SP

PUSH qq

Operation: (SP-2) ← qqL, (SP-1) ← qqH

Op Code: PUSH

Operands: qq

1	1	q	q	0	1	0	1

Description: The contents of the register pair qq are pushed to the external memory LIFO (last-in, first-out) Stack. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first decrements SP and loads the high order byte of register pair qq to the memory address specified by the SP. The SP is decremented again and loads the low order byte of qq to the memory location corresponding to this new address in the SP. The operand qq identifies register pair BC, DE, HL, or AF, assembled as follows in the object code:

Pair	qq
BC	00
DE	01
HL	10
AF	11

M Cycles	T States	4 MHz E.T.
3	11 (5, 3, 3)	2.75

Złóż na stosie parę rejestrów qq

PUSH IX

Operation: (SP-2) ← IXL, (SP-1) ← IXH

Op Code: PUSH

Operands: IX

1	1	0	1	1	1	0	1	DD
1	1	1	0	0	1	0	1	E5

Description: The contents of the Index Register IX are pushed to the external memory LIFO (last-in, first-out) Stack. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first decrements SP and loads the high order byte of IX to the memory address specified by SP; then decrements SP again and loads the low order byte to the memory location corresponding to this new address in SP.

M Cycles	T States	4 MHz E.T.
4	15 (4, 5, 3, 3)	3.75

Złóż na stosie rejestr IX

PUSH IY

Operation: (SP-2) ← IYL, (SP-1) ← IYH

Op Code: PUSH

Operands: IY

1	1	1	1	1	1	0	1	FD
1	1	1	0	0	1	0	1	E5

Description: The contents of the Index Register IY are pushed to the external memory LIFO (last-in, first-out) Stack. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first decrements the SP and loads the high order byte of IY to the memory address specified by SP; then decrements SP again and loads the low order byte to the memory location corresponding to this new address in SP.

M Cycles	T States	4 MHz E.T.
4	15 (4, 5, 3, 3)	3.75

Złóż na stosie rejestr IY

POP qq

Operation: qqH ← (SP+1), qqL ← (SP)

Op Code: POP

Operands: qq

1	1	q	q	0	0	0	1

Description: The top two bytes of the external memory LIFO (last-in, first-out) Stack are popped to register pair qq. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first loads to the low order portion of qq, the byte at memory location corresponding to the contents of SP; then SP is incriminated and the contents of the corresponding adjacent memory location are loaded to the high order portion of qq and the SP is now incriminated again. The operand qq identifies register pair BC, DE, HL, or AF, assembled as follows in the object code:

Pair	r
BC	00
DE	01
HL	10
AF	11

M Cycles	T States	4 MHz E.T.
3	10 (4, 3, 3)	2.50

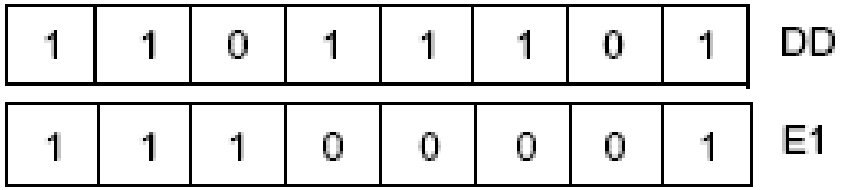
Ściągnij ze stosu dane do pary rejestrów qq

POP IX

Operation: IXH ← (SP+1), IXL ← (SP)

Op Code: POP

Operands: IX



Description: The top two bytes of the external memory LIFO (last-in, first-out) Stack are popped to Index Register IX. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first loads to the low order portion of IX the byte at the memory location corresponding to the contents of SP; then SP is incremented and the contents of the corresponding adjacent memory location are loaded to the high order portion of IX. The SP is incremented again.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

Condition Bits Affected: None

Ściągnij ze stosu daną do rejestru IX

POP IY

Operation: IYH ← (SP-X1), IYL ← (SP)

Op Code: POP

Operands: IY

1	1	0	1	1	1	0	1	DD
1	1	1	1	1	1	0	1	FD

Description: The top two bytes of the external memory LIFO (last-in, first-out) Stack are popped to Index Register IY. The Stack Pointer (SP) register pair holds the 16-bit address of the current top of the Stack. This instruction first loads to the low order portion of IY the byte at the memory location corresponding to the contents of SP; then SP is incremented and the contents of the corresponding adjacent memory location are loaded to the high order portion of IY. The SP is incremented again.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

Ściągnij ze stosu daną do rejestru IY

EX DE, HL

Operation: DE ↔ HL

Op Code: EX

Operands: DE, HL

1	1	1	0	1	0	1	1	EB

Description: The 2-byte contents of register pairs DE and HL are exchanged.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Condition Bits Affected: None

Wymień zawartość pary rejestrów DE z HL

EX AF, AF'

Operation: AF ↔ AF'

Op Code: EX

Operands: AF, AF'

0	0	0	0	1	0	0	0	08

Description: The 2-byte contents of the register pairs AF and AF are exchanged.

Register pair AF consists of registers A' and F'.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Wymień zawartość pary rejestrów AF z A’F’

EXX

Operation: (BC) ↔ (BC'), (DE) ↔ (DE'), (HL) ↔ (HL')

Op Code: EXX

Operands: —

1	1	0	1	1	0	0	0	D9

Description: Each 2-byte value in register pairs BC, DE, and HL is exchanged with the 2-byte value in BC', DE', and HL', respectively.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Wymień zawartość pary rejestrów BC z B’C’, DE z D’E’, HL z H,L,

EX (SP), HL

Operation: H ↔ (SP+1), L ↔ (SP)

Op Code: EX

Operands: (SP), HL

1	1	1	0	0	0	1	1	E3

Description: The low order byte contained in register pair HL is exchanged with the contents of the memory address specified by the contents of register pair SP (Stack Pointer), and the high order byte of HL is exchanged with the next highest memory address (SP+1).

M Cycles	T States	4 MHz E.T.
5	19 (4, 3, 4, 3, 5)	4.75

Wymień zawartość komórek pamięci o adresie wskazywanym przez wskaźnik stosu z zawartością HL

EX (SP), IX

Operation: IXH ↔ (SP+1), IXL ↔ (SP)

Op Code: EX

Operands: (SP), IX

1	1	0	1	1	1	0	1	DD
1	1	1	0	0	0	1	1	E3

Description: The low order byte in Index Register IX is exchanged with the contents of the memory address specified by the contents of register pair SP (Stack Pointer), and the high order byte of IX is exchanged with the next highest memory address (SP+1).

M cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 4, 3, 5)	5.75

Wymień zawartość komórek pamięci o adresie wskazywanym prze wskaźnik stosu z zawartością IX

EX (SP), IY

Operation: IYH ↔ (SP+1), IYL ↔ (SP)

Op Code: EX

Operands: (SP), IY

1	1	1	1	1	1	0	1	FD
1	1	1	0	0	0	1	1	E3

Description: The low order byte in Index Register IY is exchanged with the contents of the memory address specified by the contents of register pair SP (Stack Pointer), and the high order byte of IY is exchanged with the next highest memory address (SP+1).

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 4, 3, 5)	5.75

Wymień zawartość komórek pamięci o adresie wskazywanym prze wskaźnik stosu z zawartością IY

Instrukcje arytmetyczne 8-mio bitowe

ADD A, r

Operation: A ← A + r

Op Code: ADD

Operands: A, r

Description: The contents of register r are added to the contents of the Accumulator, and the result is stored in the Accumulator. The symbol r identifies the registers A, B, C, D, E, H, or L, assembled as follows in the object code:

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
1	4	1.00

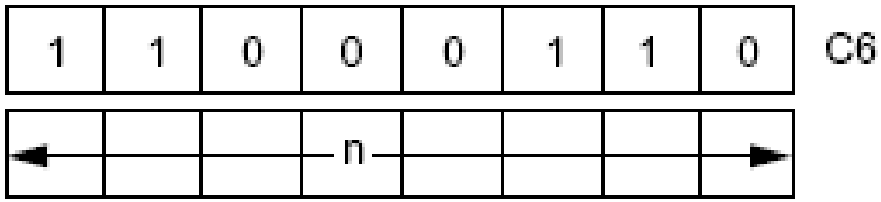
Dodaj do zawartości A zawartość innego rejestru, wynik umieść w A

ADD A, n

Operation: $A \leftarrow A + n$

Op Code: ADD

Operands: A, n



Description: The integer n is added to the contents of the Accumulator, and the results are stored in the Accumulator.

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

Dodaj do zawartości A liczbę 8-mio bitową, wynik umieść w A

ADD A, (HL)

Operation: A ← A + (HL)

Op Code: ADD

Operands: A, (HL)

1	0	0	0	0	1	1	0	86

Description: The byte at the memory address specified by the contents of the HL register pair is added to the contents of the Accumulator, and the result is stored in the Accumulator.

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

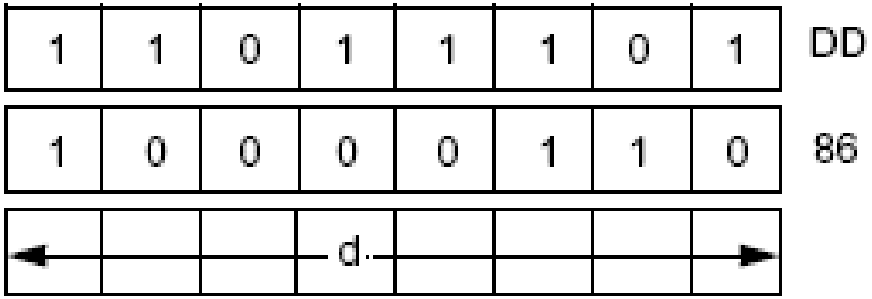
Dodaj do zawartości A zawartość komórki pamięci o adresie zawartym w HL, wynik umieść w A

ADD A, (IX + d)

Operation: $A \leftarrow A + (IX+d)$

Op Code: ADD

Operands: A, (IX + d)



Description: The contents of the Index Register (register pair IX) is added to a two's complement displacement d to point to an address in memory. The contents of this address is then added to the contents of the Accumulator and the result is stored in the Accumulator.

M Cycles	T States	4 MHz E.T.
5	19 (4, 4, 3, 5, 3)	4.75

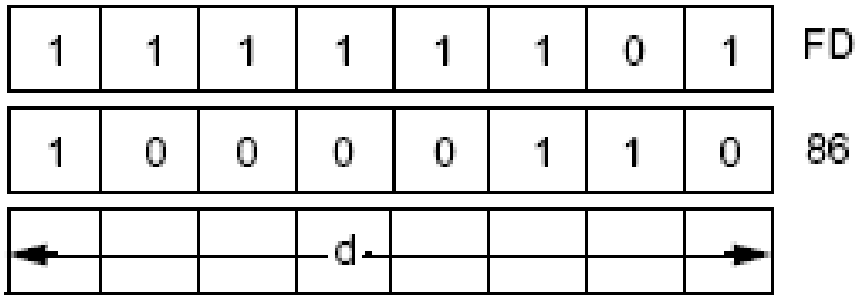
Dodaj do zawartości A zawartość komórki pamięci o adresie zawartym w IX z offsetem d, wynik umieść w A

ADD A, (IY + d)

Operation: $A \leftarrow A + (ID+d)$

Op Code: ADD

Operands: A, (IY + d)



Description: The contents of the Index Register (register pair IY) is added to a two's complement displacement d to point to an address in memory. The contents of this address is then added to the contents of the Accumulator, and the result is stored in the Accumulator.

M Cycles	T States	4 MHz E.T.
5	19(4, 4, 3, 5, 3)	4.75

Dodaj do zawartości A zawartość komórki pamięci o adresie zawartym w IY z offsetem d, wynik umieść w A

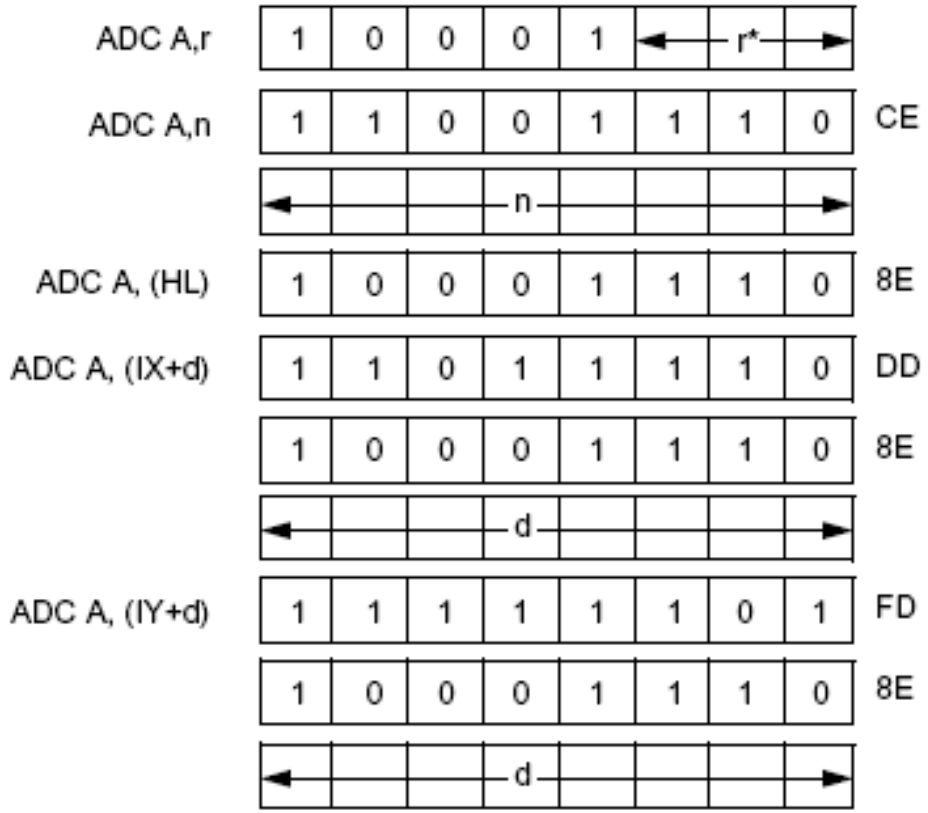
ADC A, s

Operation: $A \leftarrow A + s + CY$

Op Code: ADC

Operands: A, s

This s operand is any of r, n, (HL), (IX+d), or (IY+d) as defined for the analogous ADD instruction. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Dodaj do zawartości A zawartość: rejestru, liczbę n, zawartość komórki pamięci adresowanej przez HL, IX, IY oraz znacznika C, wynik w A

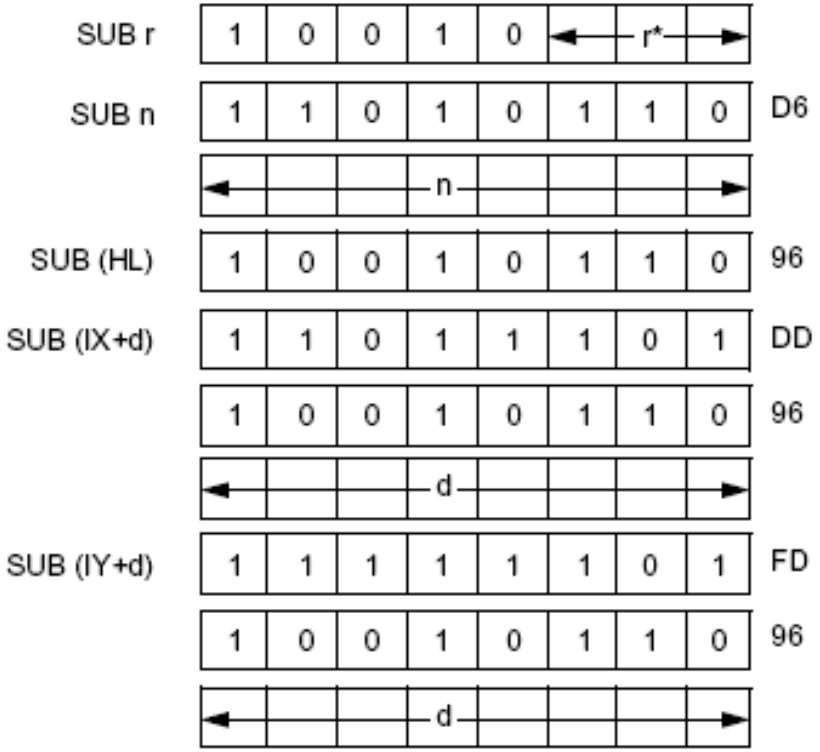
SUB s

Operation: A ← A - s

Op Code: SUB

Operands: s

This s operand is any of r, n, (HL), (IX+d), or (IY+d) as defined for the analogous ADD instruction. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Odejmij od zawartości A zawartość: rejestru, liczbę n, zawartość komórki pamięci adresowanej przez HL, IX, IY, wynik w A

SBC A, s

Operation: A ← A - s - CY

Op Code: SBC

Operands: A, s

The s operand is any of r, n, (HL), (IX+d), or (IY+d) as defined for the analogous ADD instructions. These possible Op Code/operand combinations are assembled as follows in the object code:

SBC A, r	1	0	0	1	1	←	r*	→
SBC A, n	1	1	0	1	1	1	1	0	DE
	←			n				→
SBC A, (HL)	1	0	0	1	1	1	1	0	9E
SBC A, (IX+d)	1	1	0	1	1	1	0	1	DD
	1	0	0	1	1	1	1	0	9E
	←			d				→
SBC A, (IY+d)	1	1	1	1	1	1	0	1	FD
	1	0	0	1	1	1	1	0	9E
	←			d				→

Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Odejmij od zawartości A zawartość: rejestru, liczbę n, zawartość komórki pamięci adresowanej przez HL, IX, IY oraz znacznika C, wynik w A

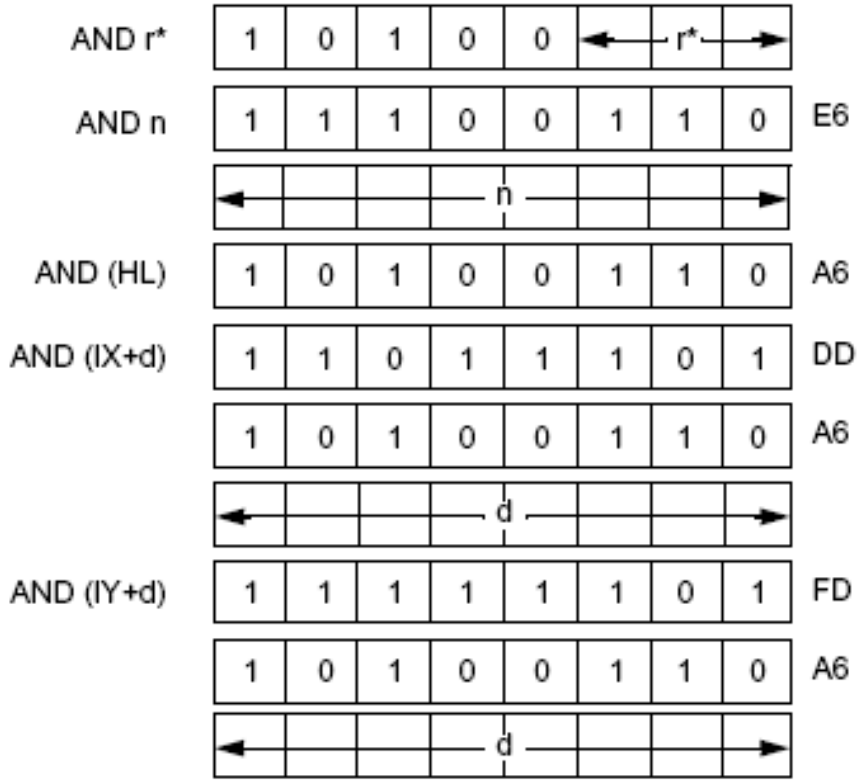
AND s

Operation: $A \leftarrow A \wedge s$

Op Code: AND

Operands: s

The s operand is any of r, n, (HL), (IX+d), or (IY+d), as defined for the analogous ADD instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Wymnóż logicznie zawartość A z zawartością: rejestru, liczbą n, zawartością komórki pamięci adresowanej przez HL, IX, IY, wynik w A

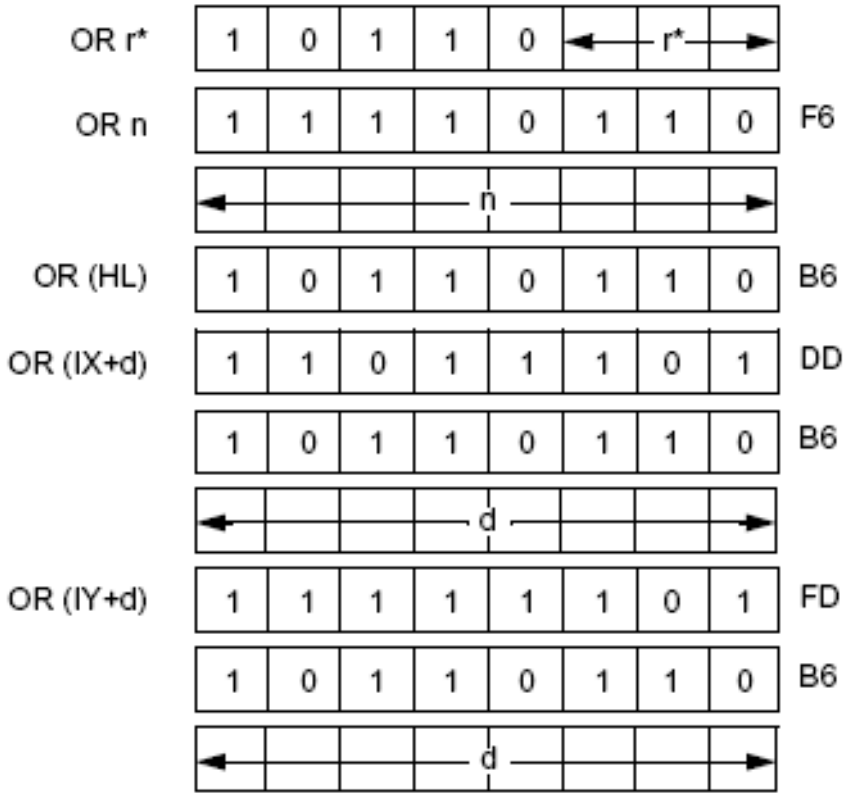
OR s

Operation: $A \leftarrow A \vee s$

Op Code: OR

Operands: s

The s operand is any of r, n, (HL), (IX+d), or (IY+d), as defined for the analogous ADD instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Dodaj logicznie zawartość A z zawartością: rejestru, liczbą n, zawartością komórki pamięci adresowanej przez HL, IX, IY, wynik w A

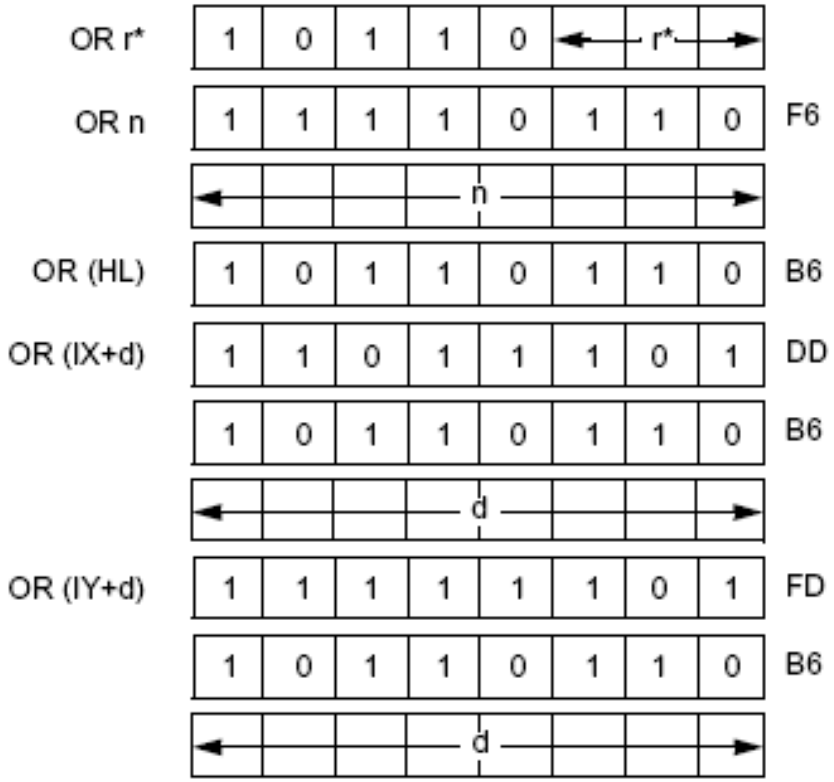
XOR s

Operation: $A \leftarrow A \oplus s$

Op Code: XOR

Operands: s

The s operand is any of r, n, (HL), (IX+d), or (IY+d), as defined for the analogous ADD instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Wykonaj operację XOR zawartości A z zawartością: rejestru, liczbą n, zawartością komórki pamięci adresowanej przez HL, IX, IY, wynik w A

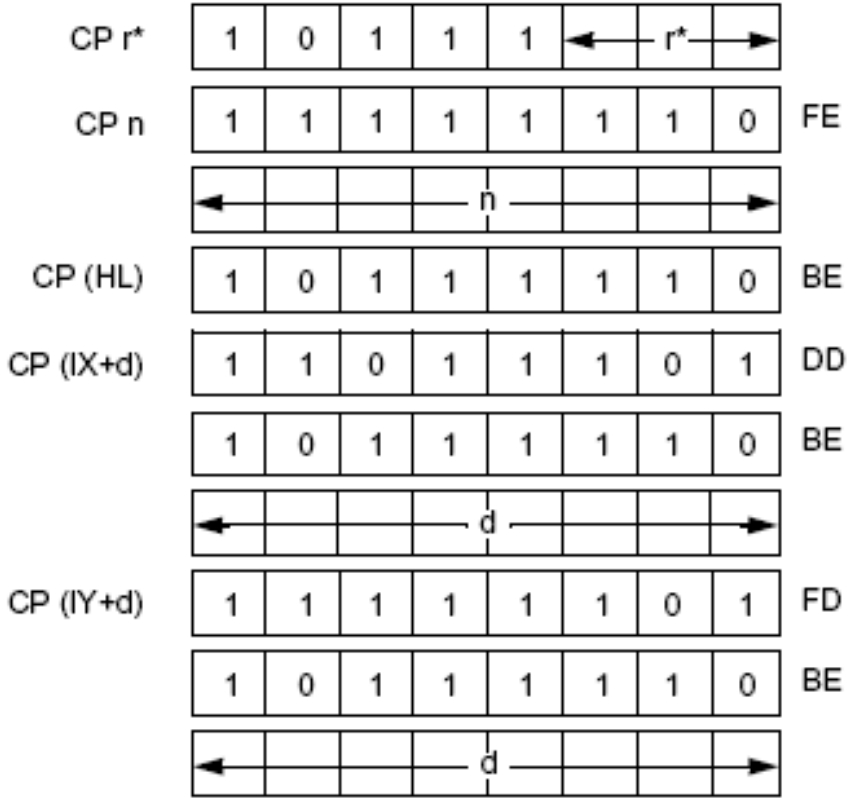
CP s

Operation: A - s

Op Code: CP

Operands: s

The s operand is any of r, n, (HL), (IX+d), or (IY+d), as defined for the analogous ADD instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

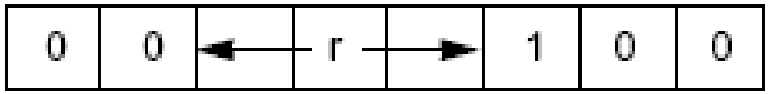
Porównaj zawartość A z zawartością: rejestru, liczbą n, zawartością komórki pamięci adresowanej przez HL, IX, IY, wyniku nie zapisuj

INC r

Operation: r ← r + 1

Op Code: INC

Operands: r



Description: Register r is incremented and register r identifies any of the registers A, B, C, D, E, H, or L, assembled as follows in the object code.

Register	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

M Cycles	T States	4 MHz E.T.
1	4	1.00

Zwiększ o 1 zawartość rejestru r

INC (HL)

Operation: (HL) ← (HL) + 1

Op Code: INC

Operands: (HL)

0	0	1	1	0	1	0	0	34

Description: The byte contained in the address specified by the contents of the HL register pair is incremented.

M Cycles	T States	4 MHz E.T.
3	11 (4, 4, 3)	2.75

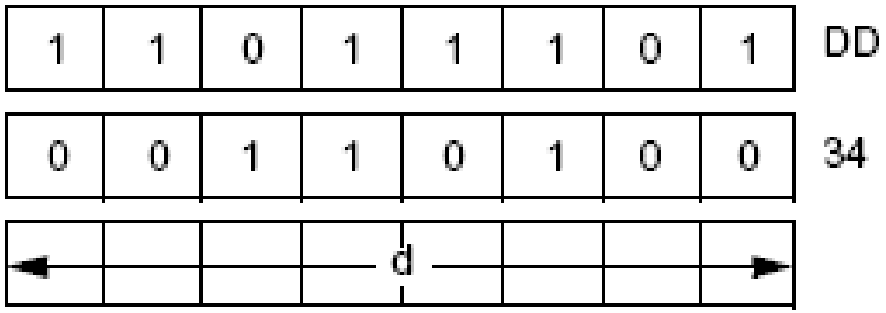
Zwiększ o 1 zawartość komórki pamięci o adresie zawartym w parze rejestrów HL

INC (IX+d)

Operation: (IX+d) ← (IX+d) + 1

Op Code: INC

Operands: (IX+d)



Description: The contents of the Index Register IX (register pair IX) are added to a two's complement displacement integer d to point to an address in memory. The contents of this address are then incremented.

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75

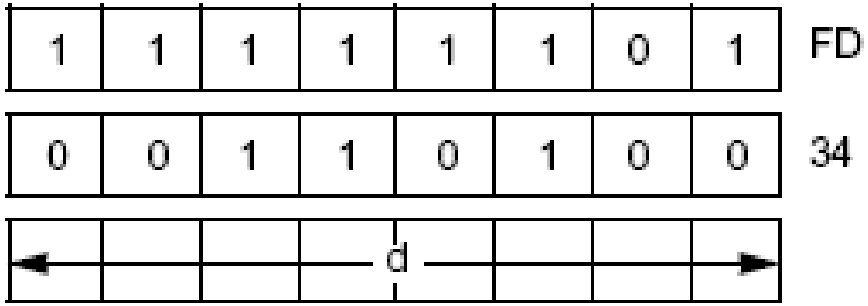
Zwiększ o 1 zawartość komórki pamięci o adresie zawartym IX z offsetem d

INC (IY+d)

Operation: (IY+d) ← (IY+d) + 1

Op Code: INC

Operands: (IY+d)



Description: The contents of the Index Register IY (register pair IY) are added to a two's complement displacement integer d to point to an address in memory. The contents of this address are then incremented.

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75

Zwiększ o 1 zawartość komórki pamięci o adresie zawartym IY z offsetem d

DEC m

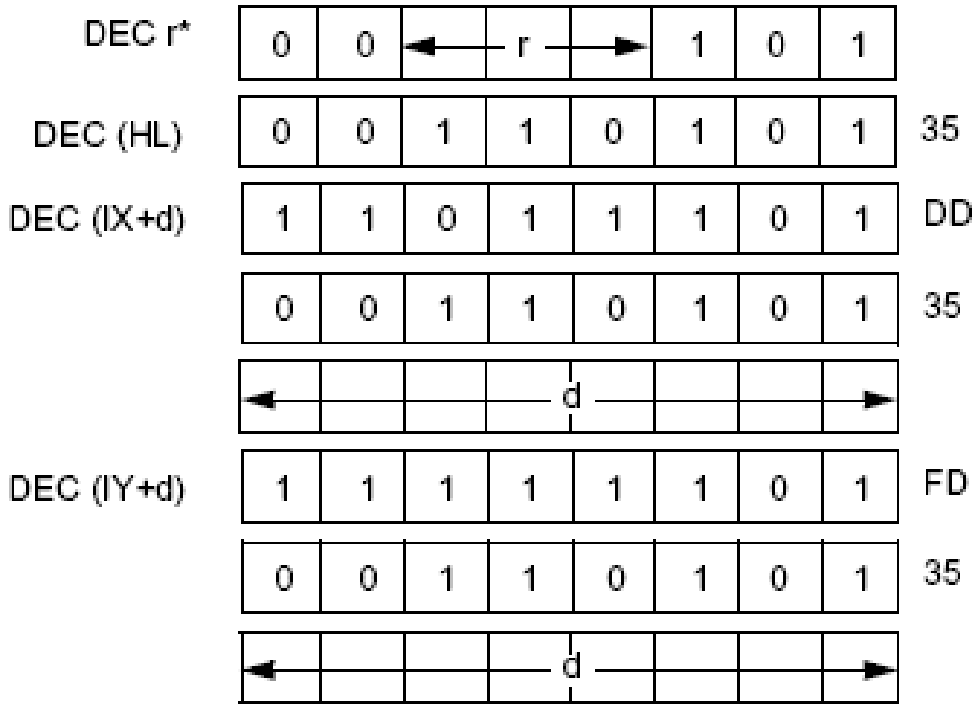
Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

Operation: m ← m- 1

Op Code: DEC

Operands: m

The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous INC instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Zmniejsz o 1 zwartość rejestru r, komórki pamięci o adresie zawartym w HL, o adresie zwartym w IX lub IY z offsetem d

Rozkazy arytmetyczne ogólnego przeznaczenia oraz sterujące CPU

DAA

Operation:

Op Code: DAA

0	0	1	0	0	1	1	1	27

M Cycles	T States	4 MHz E.T.
1	4	1.00

Korekcja dziesiętna po dodawaniu i odejmowaniu

Operation	C Before DAA	Hex Value In Upper Digit (bit 7-4)	H Before DAA	Hex Value In Lower Digit (bit 3-0)	Number Added To Byte	C After DAA
	0	9-0	0	0-9	00	0
	0	0-8	0	A-F	06	0
	0	0-9	1	0-3	06	0
ADD	0	A-F	0	0-9	60	1
ADC	0	9-F	0	A-F	66	1
INC	0	A-F	1	0-3	66	1
	1	0-2	0	0-9	60	1
	1	0-2	0	A-F	66	1
	1	0-3	1	0-3	66	1
SUB	0	0-9	0	0-9	00	0
SBC	0	0-8	1	6-F	FA	0
DEC	1	7-F	0	0-9	A0	1
NEG	1	6-7	1	6-F	9A	1

Przykłady korekcji dziesiętnej

CPL

Operation: $A \leftarrow \overline{A}$

Op Code: CPL

0	0	1	0	1	1	1	1	2F

Description: The contents of the Accumulator (register A) are inverted (one's complement).

M Cycles	T States	4 MHz E.T.
1	4	1.00

Zanegowanie zawartości akumulatora

NEG

Operation: A ← 0 - A

Op Code: NEG

1	1	1	0	1	1	0	1	ED
0	1	0	0	0	1	0	0	44

Description: The contents of the Accumulator are negated (two's complement). This is the same as subtracting the contents of the Accumulator from zero. Note that 80H is left unchanged.

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

Example: If the contents of the Accumulator are

1	0	0	1	1	0	0	0

at execution of `NEG` the Accumulator contents are

0	1	1	0	1	0	0	0

Negacja zawartości akumulatora

CCF

Operation: $CY \leftarrow \overline{CY}$

Op Code: CCF

0	0	1	1	1	1	1	1	3F

Description: The Carry flag in the F register is inverted.

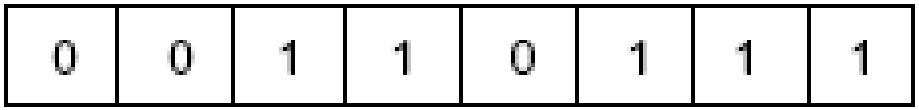
M Cycles	T States	4 MHz E.T.
1	4	1.00

Negacja bitu przeniesienia

SCF

Operation: CY ← 1

Op Code: SCF



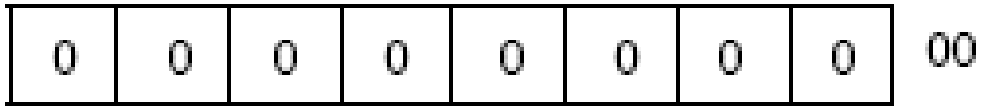
Description: The Carry flag in the F register is set.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Ustawienie bitu przeniesienia

Operation: —

Op Code: NOP



Description: The CPU performs no operation during this machine cycle.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Operacja pusta (No operating) nic nie rób

HALT

Operation: —

Op Code: HALT

0	1	1	1	0	1	1	0

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Description: The HALT instruction suspends CPU operation until a subsequent interrupt or reset is received. While in the HALT state, the processor executes NOPs to maintain memory refresh logic.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Rozkaz zatrzymania (oczekiwania na przerwanie)

DI

Operation: IFF ← 0

Op Code: DI

1	1	1	1	0	0	1	1	F3

Description: DI disables the maskable interrupt by resetting the interrupt enable flip-flops (IFF1 and IFF2). Note that this instruction disables the maskable interrupt during its execution.

M cycles	T States	4 MHz E.T.
1	4	1.00

Zamaskowanie przerwań maskowalnych

EI

Operation: IFF ← 1

Op Code: EI

1	1	1	1	1	0	1	1	FB

Description: The enable interrupt instruction sets both interrupt enable flip flops (IFFI and IFF2) to a logic 1, allowing recognition of any maskable interrupt. Note that during the execution of this instruction and the following instruction, maskable interrupts are disabled.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Odmaskowanie przerwań maskowalnych

IM 0

Operation: —

Op Code: IM

Operands: 0

1	1	1	0	1	1	0	1	ED
0	1	0	0	0	1	1	0	46

Description: The IM 0 instruction sets interrupt mode 0. In this mode, the interrupting device can insert any instruction on the data bus for execution by the CPU. The first byte of a multi-byte instruction is read during the interrupt acknowledge cycle. Subsequent bytes are read in by a normal memory read sequence.

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

Aktywacja modu 0 przyjęcia przerwań maskowalnych

IM 1

Operation: —

Op Code: IM

Operands: 1

1	1	1	0	1	1	0	1	ED
0	1	0	1	0	1	1	0	56

Description: The IM 1 instruction sets interrupt mode 1. In this mode, the processor responds to an interrupt by executing a restart to location 0038H.

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

Aktywacja modu 1 przyjęcia przerwań maskowalnych

IM 2

Operation: —

Op Code: IM

Operands: 2

1	1	1	0	1	1	0	1	ED
0	1	0	1	1	1	1	0	5E

Description: The IM 2 instruction sets the vectored interrupt mode 2. This mode allows an indirect call to any memory location by an 8-bit vector supplied from the peripheral device. This vector then becomes the least-significant eight bits of the indirect pointer, while the I register in the CPU provides the most-significant eight bits. This address points to an address in a vector table that is the starting address for the interrupt service routine.

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

Aktywacja modu 2 przyjęcia przerwań maskowalnych

Rozkazy arytmetyczne 16-to bitowe

ADD HL, ss

Operation: HL ← HL + ss

Op Code: ADD

Operands: HL, ss

0	0	s	s	1	0	0	1

Description: The contents of register pair ss (any of register pairs BC, DE, HL, or SP) are added to the contents of register pair HL and the result is stored in HL. Operand ss is specified as follows in the assembled object code.

Register Pair	ss
BC	00
DE	01
HL	10
SP	11

M Cycles	T States	4 MHz E.T.
3	11 (4, 4, 3)	2.75

Do zawartości HL dodaj zawartości pary rejestrów ss, wynik w HL

ADC HL, ss

Operation: HL ← HL + ss + CY

Op Code: ADC

Operands: HL, ss

1	1	1	0	1	1	0	1	ED
0	1	s	s	1	0	1	0	

Description: The contents of register pair ss (any of register pairs BC, DE, HL, or SP) are added with the Carry flag (C flag in the F register) to the contents of register pair HL, and the result is stored in HL. Operand ss is specified as follows in the assembled object code.

Register Pair	ss
BC	00
DE	01
HL	10
SP	11

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Do zawartości HL dodaj zawartości pary rejestrów ss oraz bitu C, wynik w HL

SBC HL, ss

Operation: HL ← HI - ss - CY

Op Code: SBC

Operands: HL, ss

1	1	1	0	1	1	0	1	ED
0	1	s	s	0	0	1	0	

Description: The contents of the register pair ss (any of register pairs BC, DE, HL, or SP) and the Carry Flag (C flag in the F register) are subtracted from the contents of register pair HL, and the result is stored in HL. Operand ss is specified as follows in the assembled object code.

Register Pair	ss
BC	00
DE	01
HL	10
SP	11

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Odejmij od zawartości HL zawartość pary rejestrów ss oraz bitu C, wynik w HL

ADD IX, pp

Operation: IX ← IX + pp

Op Code: ADD

Operands: IX, pp

1	1	0	1	1	1	0	1	DD
0	0	p	p	1	0	0	1	

Description: The contents of register pair pp (any of register pairs BC, DE, IX, or SP) are added to the contents of the Index Register IX, and the results are stored in IX. Operand pp is specified as follows in the assembled object code.

Register Pair	pp
BC	00
DE	01
IX	10
SP	11

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Dodaj do zawartości rejestru IX zawartość pary rejestrów pp

ADD IY, rr

Operation: IY ← IY + rr

Op Code: ADD

Operands: IY, rr

1	1	1	1	1	1	0	1	FD
0	0	r	r	1	0	0	1	

Description: The contents of register pair rr (any of register pairs BC, DE, IY, or SP) are added to the contents of Index Register IY, and the result is stored in IY. Operand rr is specified as follows in the assembled object code.

Register Pair	rr
BC	00
DE	01
IY	10
SP	11

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Dodaj do zawartości rejestru IY zawartość pary rejestrów rr

INC ss

Operation: ss ← ss + 1

Op Code: INC

Operands: ss

0	0	s	s	0	0	1	1

Description: The contents of register pair ss (any of register pairs BC, DE, HL, or SP) are incremented. Operand ss is specified as follows in the assembled object code.

Register Pair	ss
BC	00
DE	01
HL	10
SP	11

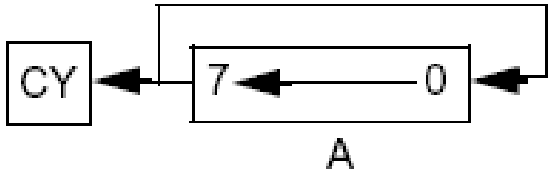
M Cycles	T States	4 MHz E.T.
1	6	1.50

Zwiększ o 1 zawartość pary rejestrów ss

Rozkazy rotacji i przesunięć

RLCA

Operation:



Op Code: RLCA

Operands: —

0	0	0	0	0	1	1	1	07

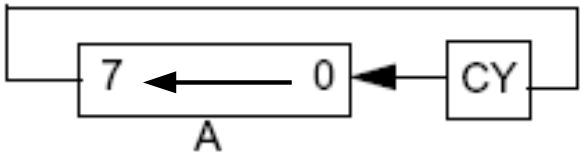
Description: The contents of the Accumulator (register A) are rotated left 1-bit position. The sign bit (bit 7) is copied to the Carry flag and also to bit 0. Bit 0 is the least-significant bit.

M cycles	T States	4 MHz E.T.
1	4	1.00

Przesuń zawartość akumulatora A o jeden bit w lewo, najstarszy bit 7 wpisz na bit 0 oraz na bit przeniesienia C

RLA

Operation:



Op Code: RLA

Operands: —

0	0	0	1	0	1	1	1

17

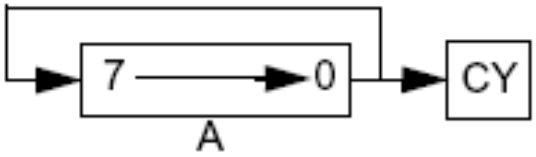
Description: The contents of the Accumulator (register A) are rotated left 1-bit position through the Carry flag. The previous content of the Carry flag is copied to bit 0. Bit 0 is the least-significant bit.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Przesuń zawartość akumulatora o jeden bit w lewo „via” bit przeniesienia C. Najstarszy bit 7 A wpisz do C, C przepisz na najmłodszy bit 0 A

RRCA

Operation:



Op Code: RRCA

Operands: —

0	0	0	0	1	1	1	1	0F

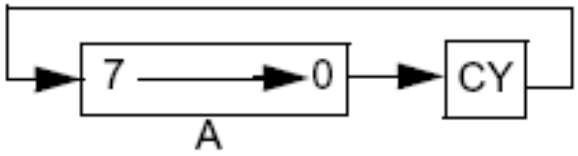
Description: The contents of the Accumulator (register A) are rotated right 1-bit position. Bit 0 is copied to the Carry flag and also to bit 7. Bit 0 is the least-significant bit.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Przesuń zawartość akumulatora A o jeden bit w prawo, najmłodszy bit wpisz na bit 7 oraz na bit przeniesienia C

RRA

Operation:



Op Code: RRA

Operands: —

0	0	0	1	1	1	1	1	1F

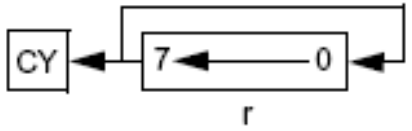
Description: The contents of the Accumulator (register A) are rotated right 1-bit position through the Carry flag. The previous content of the Carry flag is copied to bit 7. Bit 0 is the least-significant bit.

M Cycles	T States	4 MHz E.T.
1	4	1.00

Przesuń zawartość akumulatora o jeden bit w prawo „via” bit przeniesienia C. Najmłodszy bit A wpisz do C i przepisz na najstarszy bit 7 A

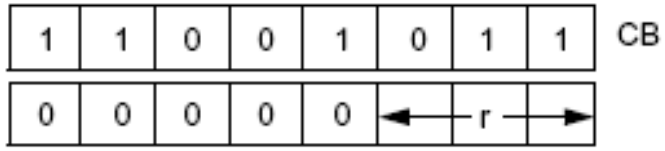
RLC r

Operation:



Op Code: RLC

Operands: r



Description: The contents of register r are rotated left 1-bit position. The content of bit 7 is copied to the Carry flag and also to bit 0. Operand r is specified as follows in the assembled object code:

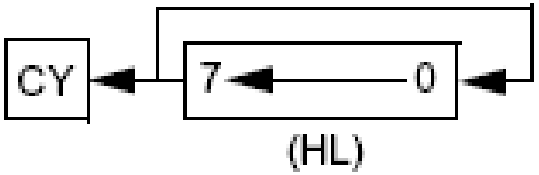
Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

Przesuń zawartość rejestru r o jeden bit w lewo, najstarszy bit 7 wpisz na bit 0 oraz na bit przeniesienia C

RLC (HL)

Operation:



Op Code: RLC

Operands: (HL)

1	1	0	0	1	0	1	1	CB
0	0	0	0	0	1	1	0	06

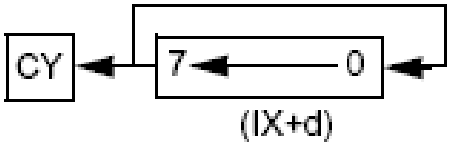
Description: The contents of the memory address specified by the contents of register pair HL are rotated left 1-bit position. The content of bit 7 is copied to the Carry flag and also to bit 0. Bit 0 is the least-significant bit.

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Przesuń zawartość komórki o adresie zawartym w HL o jeden bit w lewo, najstarszy bit 7 wpisz na bit 0 oraz na bit przeniesienia C

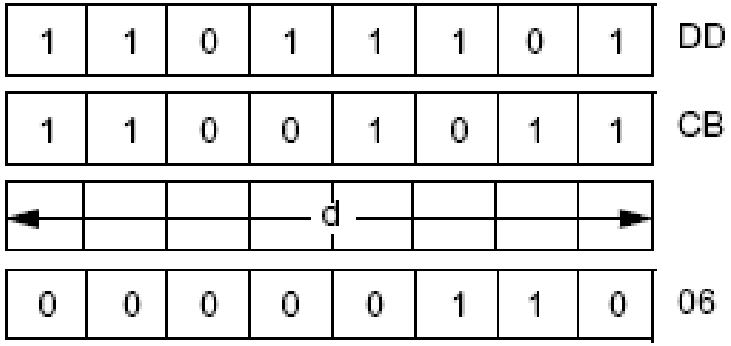
RLC (IX+d)

Operation:



Op Code: RLC

Operands: (IX+d)



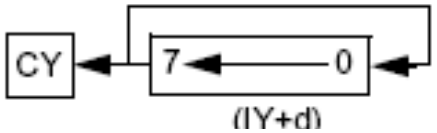
Description: The contents of the memory address specified by the sum of the contents of the Index Register IX and a two's complement displacement integer d, are rotated left 1-bit position. The content of bit 7 is copied to the Carry flag and also to bit 0. Bit 0 is the least-significant bit.

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75

Przesuń zawartość komórki o adresie zawartym w IX plus offset d o jeden bit w lewo, najstarszy bit 7 wpisz na bit 0 oraz na bit przeniesienia C

RLC (IY+d)

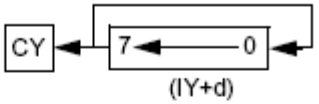
Operation:



RLC (IY+d)

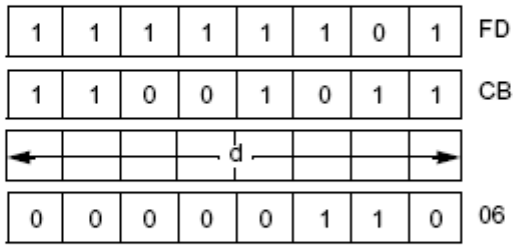
Op Code: **Operation:**

Operands:



Op Code: RLC

Operands: (IY+d)



Descriptio

Description: The contents of the memory address specified by the sum of the contents of the Index Register IY and a two's complement displacement integer d are rotated left 1-bit position. The content of bit 7 is copied to the Carry flag and also to bit 0. Bit 0 is the least-significant bit.

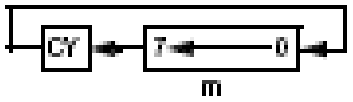
contents of
eger d are
arry flag

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75
6	23 (4, 4, 3, 5, 4, 3)	5.75

Przesuń zawartość komórki o adresie zawartym w IY plus offset d o jeden bit w lewo, najstarszy bit 7 wpisz na bit 0 oraz na bit przeniesienia C

RL m

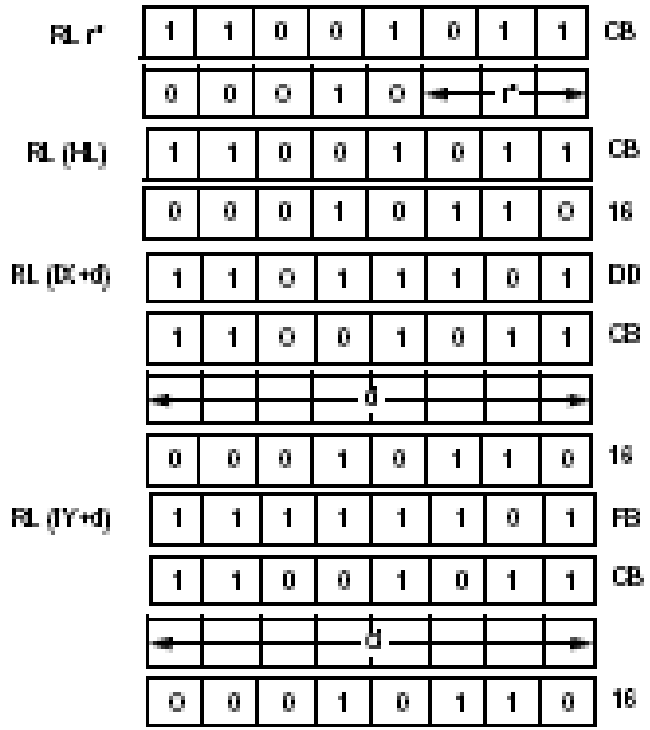
Operation:



Op Code: RL

Operands: m

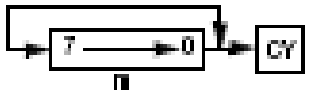
The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous RLC instructions. These possible Op Code/operand combinations are specified as follows in the assembled object code:



Przesuń zawartość rejestru r, komórki o adresie zawartej w HL, rejestrach IX, IY z offsetem d, o jeden bit w lewo „via” bit przeniesienia C. Najstarszy bit 7 wpisz do C, C przepisz na najmłodszy bit 0

RRC m

Operation:



Op Code: RRC

Operands: m

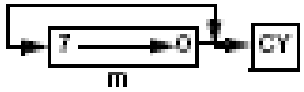
The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous RLC instructions. These possible Op Code/operand combinations are specified as follows in the assembled object code:

RRC r'	1	1	0	0	1	0	1	1	CB
	0	0	0	0	1	←	r'	→	
RRC (HL)	1	1	0	0	1	0	1	1	CB
	0	0	0	0	1	1	1	0	OE
RRC (IX+d)	1	1	0	1	1	1	0	1	DD
	1	1	0	0	1	0	1	1	CB
	←			d				→	
	0	0	0	0	1	1	1	0	OE
RRC (IY+d)	1	1	1	1	1	1	0	1	FB
	1	1	0	0	1	0	1	1	CB
	←			d				→	
	0	0	0	0	1	1	1	0	OE

Przesuń zawartość rejestru r, komórki o adresie zawartym w HL, w rejestrze IX, IY + offset d o jeden bit w prawo, najmłodszy bit wpisz na bit 7 oraz na bit przeniesienia C

RR m

Operation:



Op Code: RR

Operands: m

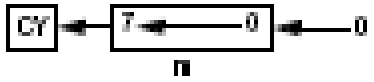
The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous RLC instructions. These possible Op Code/operand combinations are specified as follows in the assembled object code:

RR r'	1	1	0	0	1	0	1	1	CB
	0	0	0	0	1	r'			
RR (HL)	1	1	0	0	1	0	1	1	CB
	0	0	0	0	1	1	1	0	1E
RR (IX+d)	1	1	0	1	1	1	0	1	DD
	1	1	0	0	1	0	1	1	CB
	d								
	0	0	0	1	1	1	1	0	1E
RR (IY+d)	1	1	1	1	1	1	0	1	FD
	1	1	0	0	1	0	1	1	CB
	d								
	0	0	0	1	1	1	1	0	1E

Przesuń zawartość rejestru r, komórki pamięci o adresie w HL, rejestrach IX, IY + offset d, o jeden bit w prawo „via” bit przeniesienia C. Najmłodszy bit wpisz do C i przepisz na najstarszy bit 7 A

SLA m

Operation:



Op Code: SLA

Operands: m

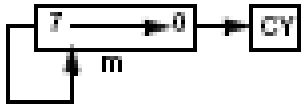
The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous RLC instructions. These possible Op Code/operand combinations are specified as follows in the assembled object code :

SLA r'	1	1	0	0	1	0	1	1	CB
	0	0	1	0	0	r'			
SLA (HL)	1	1	0	0	1	0	1	1	CB
	0	0	1	0	0	1	1	0	26
SLA (IX+d)	1	1	0	1	1	1	0	1	DD
	1	1	0	0	1	0	1	1	CB
	d								
	0	0	1	0	0	1	1	0	26
SLA (IY+d)	1	1	1	1	1	1	0	1	FD
	1	1	0	0	1	0	1	1	CB
	d								
	0	0	1	0	0	1	1	0	26

Przesuń zawartość rejestru r, komórki pamięci o adresie w HL, rejestrach IX, IY + offset d, o jeden bit w lewo. Najstarszy bit wpisz na C na najmłodszy bit wpisz 0

SRA m

Operation:



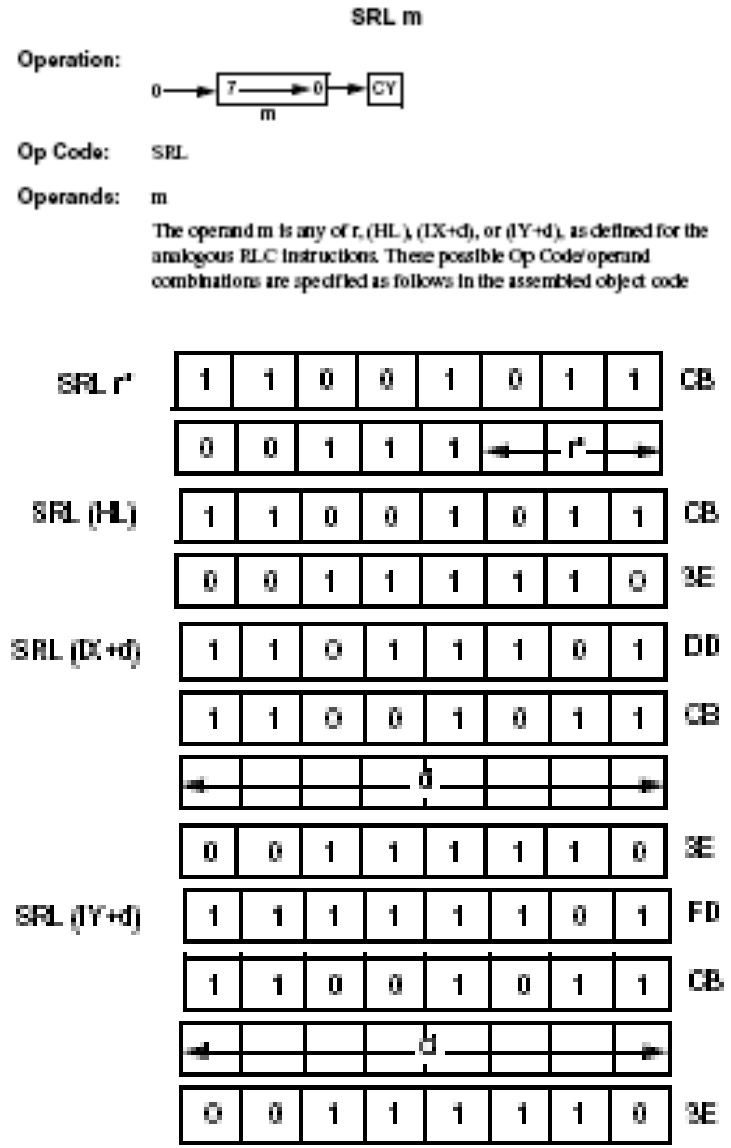
Op Code: SRA

Operands: m

The m operand is any of r, (HL), (IX+d), or (IY+d), as defined for the analogous PLC instructions. These possible Op Code/operand combinations are specified as follows in the assembled object code:

SRA r'	1	1	0	0	1	0	1	1	CB
	0	0	1	0	0	←	r'	→	
SRA(HL)	1	1	0	0	1	0	1	1	CB
	0	0	1	0	1	1	1	0	2E
SRA (IX+d)	1	1	0	1	1	1	0	1	DD
	1	1	0	0	1	0	1	1	CB
	←			d			→		
	0	0	1	0	1	1	1	0	2E
SRA(IY+d)	1	1	1	1	1	1	0	1	FD
	1	1	0	0	1	0	1	1	CB
	←			d			→		
	0	0	1	0	1	1	1	0	2E

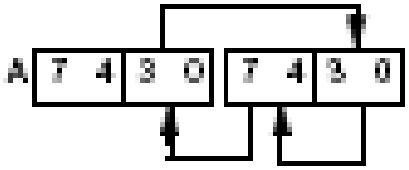
Przesuń zawartość rejestru r, komórki pamięci o adresie w HL, rejestrach IX, IY + offset d, o jeden bit w prawo. Najmłodszy bit wpisz na C na najstarszy bit przepisz jego zawartością



Przesuń zawartość rejestru r, zawartość komórki pamięci o adresie w HL, rejestrach IX, IY + offset d o jeden bit w prawo. Najmłodszy bit 0 wpisz na C, na najstarszy bit 7 wpisz 0

RLD

Operation:



Op Code: RLD

Operands: —

1	1	1	0	1	1	0	1	ED
0	1	1	0	1	1	1	1	6F

Description: The contents of the low order four bits (bits 3, 2, 1, and 0) of the memory location (HL) are copied to the high order four bits (7, 6, 5, and 4) of that same memory location; the previous contents of those high order four bits are copied to the low order four bits of the Accumulator (register A); and the previous contents of the low order four bits of the Accumulator are copied to the low order four bits of memory location (HL). The contents of the high order bits of the Accumulator are unaffected.

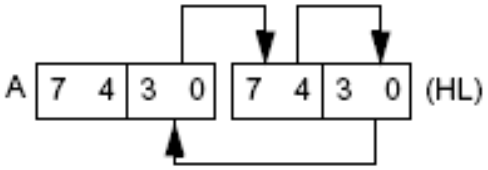
Note: (HL) means the memory location specified by the contents of the HL register pair.

M Cycles	T States	4 MHz E.T.
5	18 (4, 4, 3, 4, 3)	4.50

Cztery młodsze bity komórki pamięci o adresie zawartym w HL są kopiowane na cztery starsze bity, które wcześniej zostały skopiowane na cztery młodsze bity A, które wcześniej zostały skopiowane na cztery młodsze bity komórki o adresie w HL

RRD

Operation:



Op Code: RRD

Operands: —

1	1	1	0	1	1	0	1	ED
0	1	1	0	0	1	1	1	67

Description: The contents of the low order four bits (bits 3, 2, 1, and 0) of memory location (HL) are copied to the low order four bits of the Accumulator (register A). The previous contents of the low order four bits of the Accumulator are copied to the high order four bits (7, 6, 5, and 4) of location (HL); and the previous contents of the high order four bits of (HL) are copied to the low order four bits of (HL). The contents of the high order bits of the Accumulator are unaffected.

(HL) means the memory location specified by the contents of the HL register pair.

M Cycles	T States	4 MHz E.T.
5	18 (4, 4, 3, 4, 3)	4.50

Cztery młodsze bity komórki o adresie zawartym w HL zostają skopiowane na cztery młodsze bity A, które wcześniej zostały skopiowane na cztery starsze bity komórki o adresie w HL, które zostały wcześniej skopiowane na cztery młodsze bity tej komórki

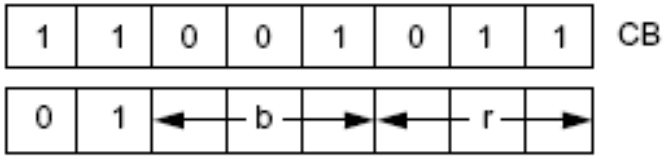
Rozkazy ustawiania, kasowania i testowania bitów

BIT b, r

Operation: $Z \leftarrow \overline{rb}$

Op Code: BIT

Operands: b, r



Description: This instruction tests bit b in register r and sets the Z flag accordingly. Operands b and r are specified as follows in the assembled object code:

Bit Tested	b	Register	r
0	000	B	000
1	001	C	001
2	010	D	010
3	011	E	011
4	100	H	100
5	101	L	101
6	110	A	111
7	111		

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	4.50

Wpisanie od znacznika Z zanegowanej wartości bitu o numerze b (0-7) w rejestrze r

BIT b, (HL)

Operation: $Z \leftarrow \overline{(HL)}b$

Op Code: BIT

Operands: b, (HL)

1	1	0	0	1	0	1	1	CB
0	1		b		1	1	0	

Description: This instruction tests bit b in the memory location specified by the contents of the HL register pair and sets the Z flag accordingly. Operand b is specified as follows in the assembled object code:

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
1	111

M Cycles	T States	4 MHz E.T.
3	12 (4, 4, 4) 4	3.00

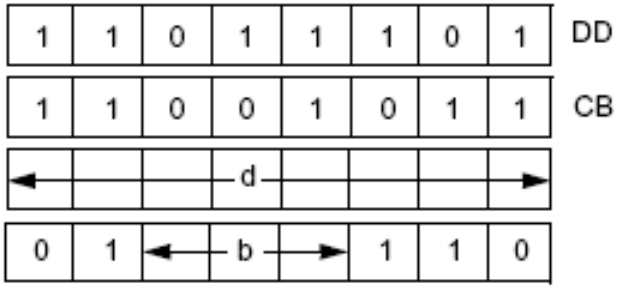
Wpisanie od znacznika Z zanegowanej wartości bitu o numerze b (0-7) w komórce pamięci o adresie zawartym w HL

BIT b, (IX+d)

Operation: $Z \leftarrow \overline{(IX+d)b}$

Op Code: BIT

Operands: b, (IX+d)



Description: This instruction tests bit b in the memory location specified by the contents of register pair IX combined with the two's complement displacement d and sets the Z flag accordingly. Operand b is specified as follows in the assembled object code.

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

M cycles	T States	4 MHz E.T.
5	20 (4, 4, 3, 5, 4)	5.00

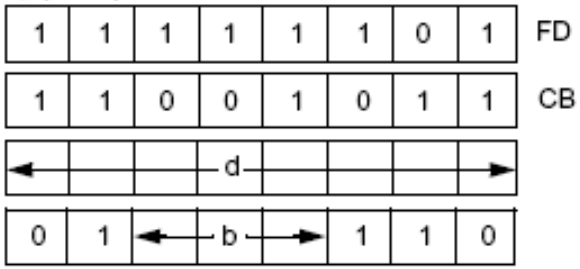
Wpisanie od znacznika Z zanegowanej wartości bitu o numerze b (0-7) w komórce pamięci o adresie zawartym w IX + offset d

BIT b, (IY+d)

Operation: $Z \leftarrow \overline{(IY+d)b}$

Op Code: BIT

Operands: b, (IY+d)



Description: This instruction tests bit b in the memory location specified by the content of register pair IY combined with the two's complement displacement d and sets the Z flag accordingly. Operand b is specified as follows in the assembled object code.

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

M Cycles	T States	4 MHz E.T.
5	20 (4, 4, 3, 5, 4)	5.00

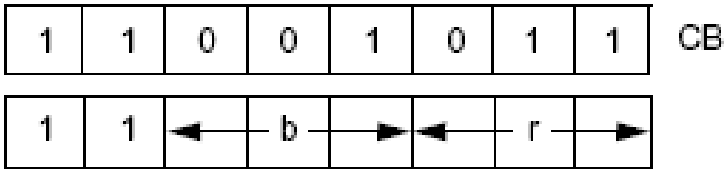
Wpisanie od znacznika Z zanegowanej wartości bitu o numerze b (0-7) w komórce pamięci o adresie zawartym w IY + offset d

SET b, r

Operation: rb ← 1

Op Code: SET

Operands: b, r



Description: Bit b in register r (any of registers B, C, D, E, H, L, or A) is set. Operands b and r are specified as follows in the assembled object code:

Bit	b	Register	r
0	000	B	000
1	001	C	001
2	010	D	010
3	011	E	011
4	100	H	100
5	101	L	101
6	110	A	111
7	111		

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

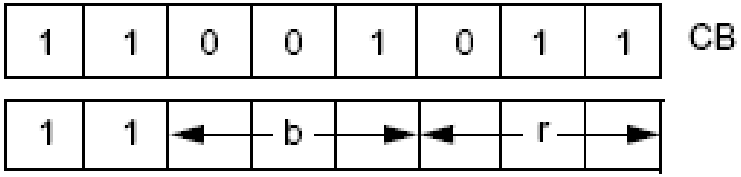
Ustawienie bitu B 90-7) w rejestrze r na „1”

SET b, (HL)

Operation: (HL)b ← 1

Op Code: SET

Operands: b, (HL)



Description: Bit b in the memory location addressed by the contents of register pair HL is set. Operand b is specified as follows in the assembled object code:

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

M Cycles	T States	4 MHz E.T.
4	15 (4, 4, 4, 3)	3.75

Ustawienie bitu b (0-7) w komórce o adresie zawartym w HL na „1”

SET b, (IX+d)

Operation: (IX+d)b ← 1

Op Code: SET

Operands: b, (IX+d)

Description: Bit b in the memory location addressed by the sum of the contents of the IX register pair and the two's complement integer d is set. Operand b is specified as follows in the assembled object code:

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75

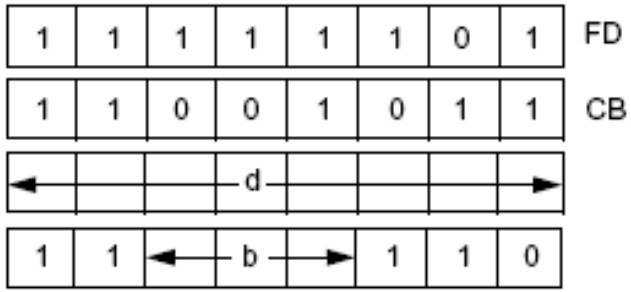
Ustawienie bitu b (0-7) w komórce o adresie zawartym w IX + offset d na „1”

SET b, (IY+d)

Operation: (IY + d) b ← 1

Op Code: SET

Operands: b, (IY + d)



Description: Bit b in the memory location addressed by the sum of the contents of the IY register pair and the two's complement displacement d is set. Operand b is specified as follows in the assembled object code:

Bit Tested	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

M Cycles	T States	4 MHz E.T.
6	23 (4, 4, 3, 5, 4, 3)	5.75

Ustawienie bitu b (0-7) w komórce o adresie zawartym w IY + offset d na „1”

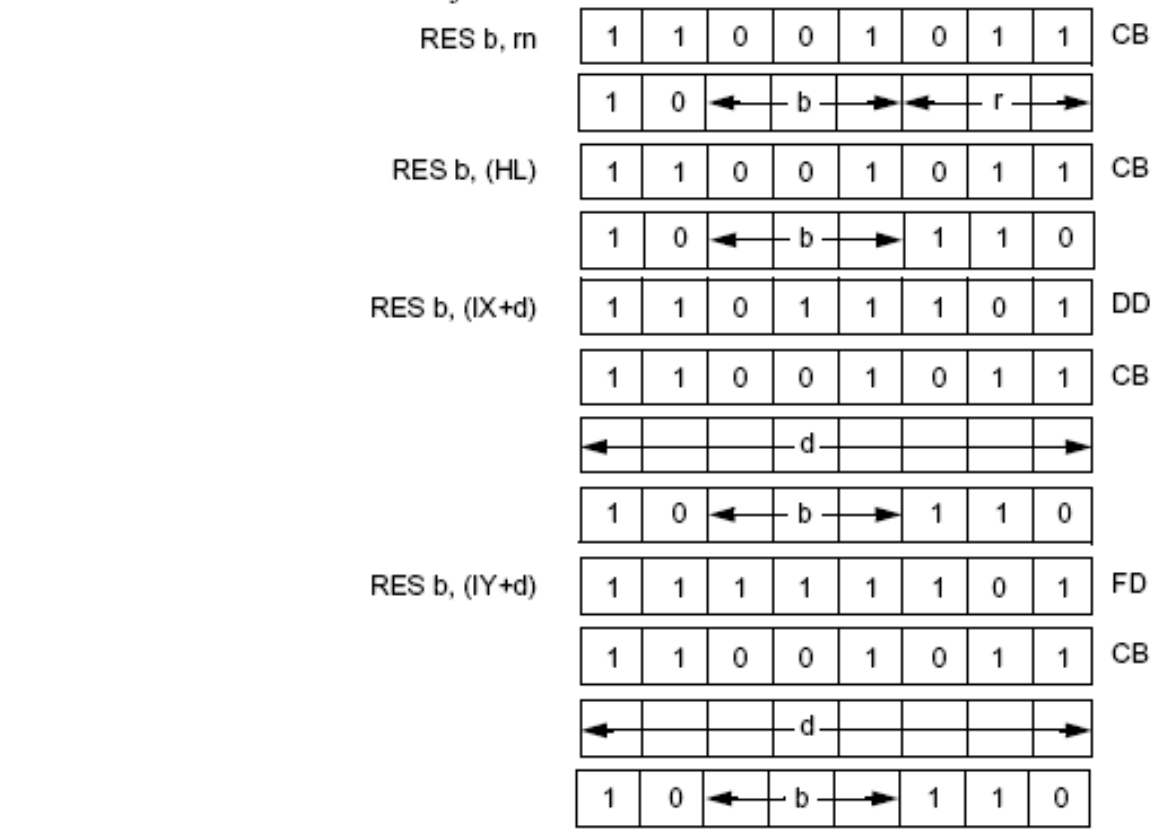
RES b, m

Operation: sb ← 0

Op Code: RES

Operands: b, m

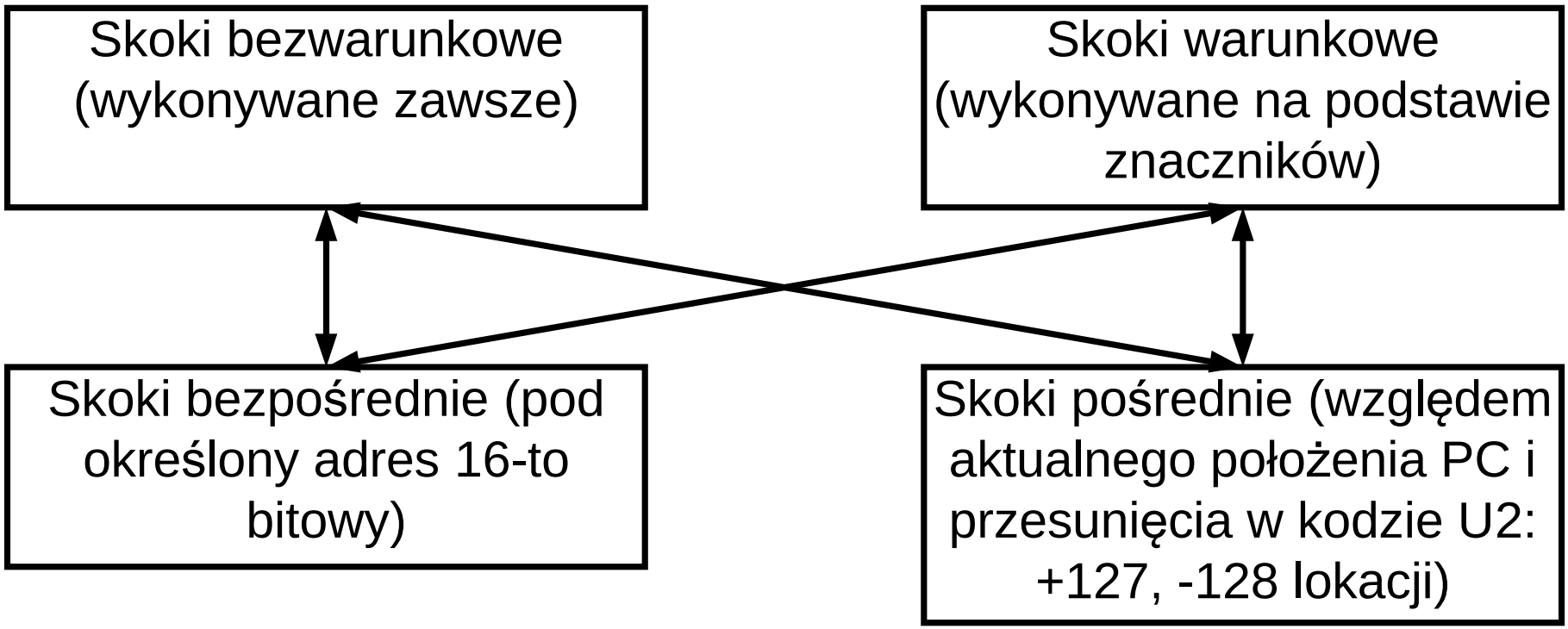
Operand b is any bit (7 through 0) of the contents of the m operand, (any of r, (HL), (IX+d), or (lY+d)) as defined for the analogous SET instructions. These possible Op Code/operand combinations are assembled as follows in the object code:



Zeruj bit b (0-7) w rejestrze r, komórce pamięci a adresie zawartym HL, rejestrach IX, IY + offset d

Rozkazy skoków

Klasyfikacja rozkazów skoków



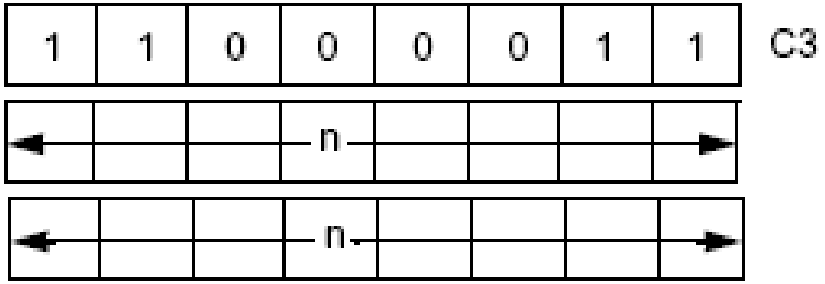
W Z80 występują wszystkie rodzaje skoków

JP nn

Operation: PC ← nn

Op Code: JP

Operands: nn



Note: The first operand in this assembled object code is the low order byte of a two-byte address.

Description: Operand nn is loaded to register pair PC (Program Counter). The next instruction is fetched from the location designated by the new contents of the PC.

M Cycles	T States	4 MHz E.T.
3	10 (4, 3, 3)	2.50

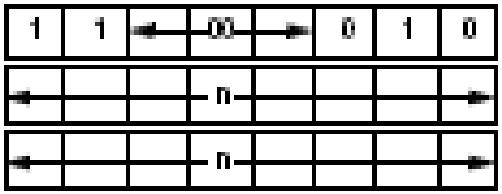
Skok bezwarunkowy, bezpośredni pod adres nn

JP cc, nn

Operation: IF cc true, PC ← nn

Op Code: JP

Operands: cc, nn



The first n operand in this assembled object code is the low-order byte of a 2-byte memory address.

Description: If condition cc is true, the instruction loads operand nn to register pair PC (Program Counter), and the program continues with the instruction beginning at address nn. If condition cc is false, the Program Counter is incremented as usual, and the program continues with the next sequential instruction. Condition cc is programmed as one of eight status that corresponds to condition bits in the Flag Register (register F). These eight status are defined in the table below that also specifies the corresponding cc bit fields in the assembled object code.

cc	Condition	Relevant Flag
000	NZ non zero	Z
001	Z zero	Z
010	NC no carry	C
011	C carry	C
100	PO parity odd	P/V
101	PE parity even	P/V
110	P sign positive	S
111	M sign negative	S

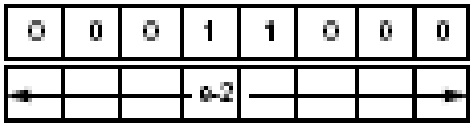
Skocz pod adres bezpośredni nn, jeśli warunek cc jest spełniony

JR e

Operation: PC ← PC + e

Op Code: JR

Operands: e



Description: This instruction provides for unconditional branching to other segments of a program. The value of the displacement e is added to the Program Counter (PC) and the next instruction is fetched from the location designated by the new contents of the PC. This jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

M Cycles	T States	4 MHz E.T.
3	12 (4, 3, 5)	3.00

Condition Bits Affected: None

Example: To jump forward five locations from address 480, the following assembly language statement is used: JR $+5

The resulting object code and final PC value is shown below:

Location	Instruction
480	18
481	03
482	-
483	-
484	-
485	← PC after jump

Skocz bezwarunkowo względem aktualnego PC o przesunięcia e (U2)

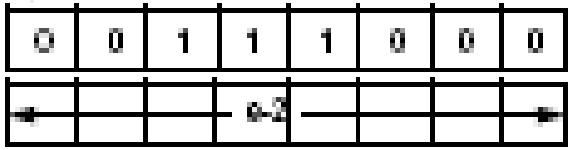
JR C, e

Operation: If C = 0, continue

If C = 1, PC ← PC+ e

Op Code: JR

Operands: C, e



Description: This instruction provides for conditional branching to other segments of a program depending on the results of a test on the Carry Flag. If the flag is equal to a 1, the value of the displacement e is added to the Program Counter (PC) and the next instruction is fetched from the location designated by the new contents of the PC. The jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

If the flag is equal to a 0, the next instruction executed is taken from the location following this instruction. If condition is met

M Cycles	T States	4 MHz E.T.
3	12 (4, 3, 5)	3.00

If condition is not met:

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

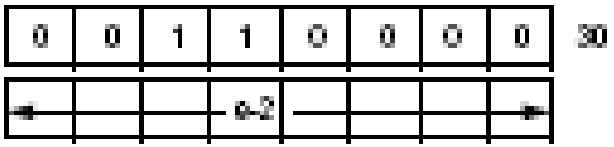
Skocz jeśli bit C=1 pod adres określony przez aktualne PC i offset e (U2)

JR NC, e

Operation: If C = 1, continue
If C = 0, PC ← PC + e

Op Code: JR

Operands: NC, e



Description: This instruction provides for conditional branching to other segments of a program depending on the results of a test on the Carry Flag. If the flag is equal to 0, the value of the displacement e is added to the Program Counter (PC) and the next instruction is fetched from the location designated by the new contents of the PC. The jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

If the flag is equal to a 1, the next instruction executed is taken from the location following this instruction.

If the condition is met:

M Cycles	T States	4 MHz E.T.
3	12 (4, 3, 5)	3.00

If the condition is not met:

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

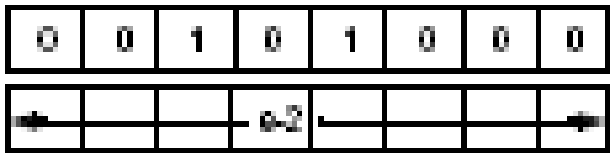
Skocz jeśli bit C=0 pod adres określony przez aktualne PC i offset e (U2)

JR Z, e

Operation: If Z = 0, continue
If Z = 1, PC ← PC + e

Op Code: JR

Operands: Z, e



Description: This instruction provides for conditional branching to other segments of a program depending on the results of a test on the Zero Flag. If the flag is equal to a 1, the value of the displacement e is added to the Program Counter (PC) and the next instruction is fetched from the location designated by the new contents of the PC. The jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

If the Zero Flag is equal to a 0, the next instruction executed is taken from the location following this instruction. If the condition is met:

M Cycles	T States	4 MHz E.T.
3	12 (4, 3, 5)	3.00

If the condition is not met;

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

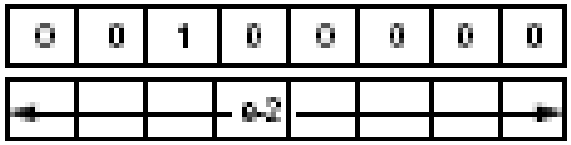
Skocz jeśli bit Z=1 pod adres określony przez aktualne PC i offset e (U2)

JR NZ, e

Operation: If Z = 1, continue
If Z = 0, PC ← pc + e

Op Code: JR

Operands: NZ, e



Description: This instruction provides for conditional branching to other segments of a program depending on the results of a test on the Zero Flag. If the flag is equal to a 0, the value of the displacement e is added to the Program Counter (PC) and the next instruction is fetched from the location designated by the new contents of the PC. The jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

If the Zero Flag is equal to a 1, the next instruction executed is taken from the location following this instruction.

If the condition is met:

M Cycles	T States	4 MHz E.T.
3	12 (4, 3, 5)	3.00

If the condition is not met:

M Cycles	T States	4 MHz E.T.
2	7 (4, 3)	1.75

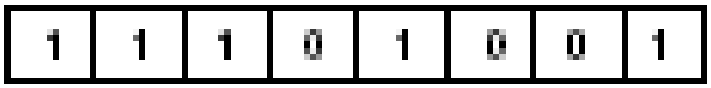
Skocz jeśli bit Z=0 pod adres określony przez aktualne PC i offset e (U2)

JP (HL)

Operation: pc ← hL

Op Code: JP

Operands: (HL)



Description: The Program Counter (register pair PC) is loaded with the contents of the HL register pair. The next instruction is fetched from the location designated by the new contents of the PC.

M Cycles	T States	4 MHz E.T.
1	4	1.00

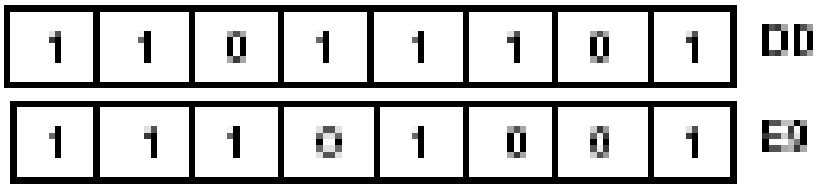
Skocz bezwarunkowo pod adres zawarty w HL

JP (IX)

Operation: pc ← IX

Op Code: JP

Operands: (IX)



Description: The Program Counter (register pair PC) is loaded with the contents of the IX Register Pair. The next instruction is fetched from the location designated by the new contents of the PC.

M Cycles	T States	4 MHz E.T.
2	*S* (4, 4)	2.00

Skocz bezwarunkowo pod adres zawarty w IX

JP (IY)

Operation: PC ← IY

Op Code: JP

Operands: (IY)

1	1	1	1	1	1	0	1	FD
1	1	1	0	1	0	0	1	E9

Description: The Program Counter (register pair PC) is loaded with the contents of the IY Register Pair. The next instruction is fetched from the location designated by the new contents of the PC.

M Cycles	T States	4 MHz E.T.
2	8 (4, 4)	2.00

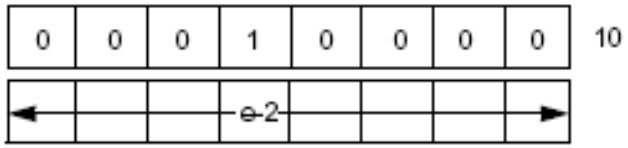
Skocz bezwarunkowo pod adres zawarty w IY

DJNZ, e

Operation: -

Op Code: DJNZ

Operands: e



Description: This instruction is similar to the conditional jump instructions except that a register value is used to determine branching. The B register is decremented, and if a non zero value remains, the value of the displacement e is added to the Program Counter (PC). The next instruction is fetched from the location designated by the new contents of the PC. The jump is measured from the address of the instruction Op Code and has a range of -126 to +129 bytes. The assembler automatically adjusts for the twice incremented PC.

If the result of decrementing leaves B with a zero value, the next instruction executed is taken from the location following this instruction.

if B ≠ 0:

M Cycles	T States	4 MHz E.T.
3	13 (5,3, 5)	3.25

If B = 0:

M Cycles	T States	4 MHz E.T.
2	8 (5, 3)	2.00

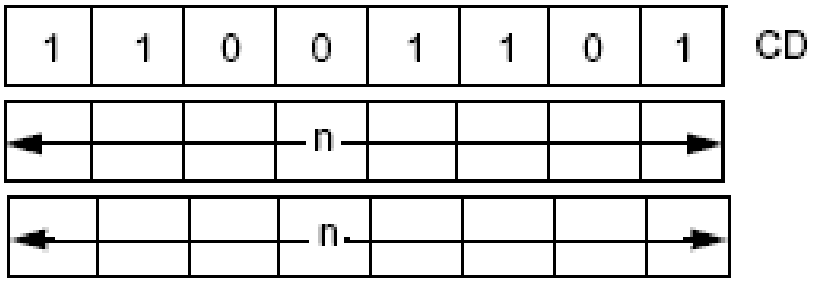
Zmniejsz zawartość rejestru B o1 i wykonaj skok względem PC z offsetem e, jeśli nie zero

CALL nn

Operation: (SP-1) ← PCH, (SP-2) ← PCL, PC ← nn

Op Code: CALL

Operands: nn



The first of the two n operands in the assembled object code above is the least-significant byte of a 2-byte memory address.

Wywołanie bezwarunkowe procedury o adresie bezpośrednim nn

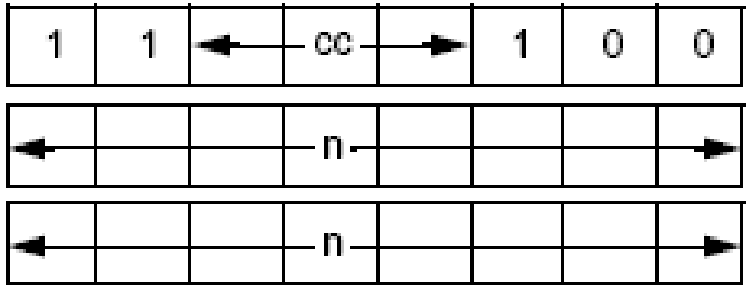
CALL cc, nn

Operation: IF cc true: (sp-1) ← PCH

(sp-2) ← PCL, pc ← nn

Op Code: CALL

Operands: cc, nn



Note: The first of the two n operands in the assembled object code above is the least-significant byte of the 2-byte memory address.

Wywołanie warunkowe procedury z adresem bezpośrednim

cc	Condition	Relevant Flag
000	NZ non zero	Z
001	Z zero	Z
010	NC non carry	C
011	C carry	Z
100	PO parity odd	P/V
101	PE parity even	P/V
110	P sign positive	S
111	M sign negative	S

Warunki wywołania

RET

Operation: pCL ← (sp), pCH ← (sp+1)

Op Code: RET

1	1	0	0	1	0	0	1	C9

Description: The byte at the memory location specified by the contents of the Stack Pointer (SP) register pair is moved to the low order eight bits of the Program Counter (PC). The SP is now incremented and the byte at the memory location specified by the new contents of this instruction is fetched from the memory location specified by the PC. This instruction is normally used to return to the main line program at the completion of a routine entered by a CALL instruction.

M Cycles	T States	4 MHz E.T.
3	10 (4, 3, 3)	2.50

Powrót bezwarunkowy z procedury

RET cc

Operation: If cc true: PCL ← (sp), pCH ← (sp+1)

Op Code: RET

Operands: cc

Powrót warunkowy z procedury

cc	Condition	Relevant Flag
000	NZ non zero	Z
001	Z zero	Z
010	NC non carry	C
011	C carry	C
100	PO parity odd	P/V
101	PE parity even	P/V
110	P sign positive	S
111	M sign negative	S

Warunki powrotu

RETI

Operation: Return from Interrupt

Op Code: RETI

1	1	1	0	1	1	0	1	ED
0	1	0	0	1	1	0	1	4D

Description: This instruction is used at the end of a maskable interrupt service routine to:

- Restore the contents of the Program Counter (PC) (analogous to the RET instruction)
- Signal an I/O device that the interrupt routine is completed. The `RETI` instruction also facilitates the nesting of interrupts, allowing higher priority devices to temporarily suspend service of lower priority service routines. However, this instruction does not enable interrupts that were disabled when the interrupt routine was entered. Before doing the `RETI` instruction, the enable interrupt instruction (`EI`) should be executed to allow recognition of interrupts after completion of the current service routine.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

Powrót z przerwania maskowalnego

RETN

Operation: Return from non maskable interrupt

Op Code: RETN

1	1	1	0	1	1	0	1	ED
0	1	0	0	0	1	0	1	45

Description: This instruction is used at the end of a non-maskable interrupts service routine to restore the contents of the Program Counter (PC) (analogous to the RET instruction). The state of IFF2 is copied back to IFF1 so that maskable interrupts are enabled immediately following the RETN if they were enabled before the nonmaskable interrupt.

M Cycles	T States	4 MHz E.T.
4	14 (4, 4, 3, 3)	3.50

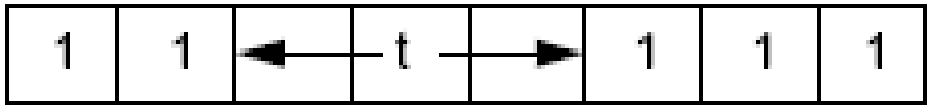
Powrót z przerwania nieaskowalnego, powoduje odtworzenie maski przerwań maskowalnych

RST p

Operation: (SP-1) ← PCH, (SP-2) ← PCL, PCH ← 0, PCL ← P

Op Code: RST

Operands: p



Rozkaz RESTARTU (0-7), powoduje złożenie na stosie adresu powrotu)

p	t
00H	000
08H	001
10H	010
18H	011
20H	100
28H	101
30H	110
38H	111

Instrukcje wejścia-wyjścia

IN A, (n)

Operation: A ← (n)

Op Code: IN

Operands: A, (n)

Description: The operand n is placed on the bottom half (A0 through A7) of the address bus to select the I/O device at one of 256 possible ports. The contents of the Accumulator also appear on the top half (A8 through A15) of the address bus at this time. Then one byte from the selected port is placed on the data bus and written to the Accumulator (register A) in the CPU.

M Cycles	T States	4 MHz LT.
3	11 (4, 3, 4)	2.75

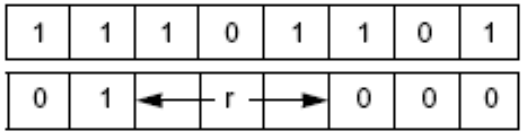
Odczyt na akumulator danej z urządzenia we-wy o adresie n

IN r (C)

Operation: r ← (C)

Op Code: IN

Operands: r, (C)



Description: The contents of register C are placed on the bottom half (A0 through A7) of the address bus to select the I/O device at one of 256 possible ports. The contents of Register B are placed on the top half (A8 through A15) of the address bus at this time. Then one byte from the selected port is placed on the data bus and written to register r in the CPU. Register r identifies any of the CPU registers shown in the following table, which also indicates the corresponding 3-bit r field for each. The flags are affected, checking the input data.

Register	r	
Flag	110	Undefined Op Code, set the flag
B	000	
C	001	
D	010	
E	011	
H	100	
L	101	
A	111	

M Cycles	T States	4 MHz E.T.
3	12 (4, 4, 4)	3.00

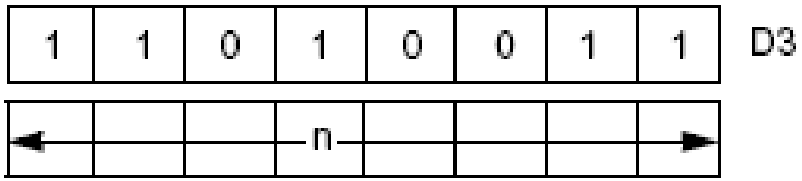
Odczyt do rejestru r danej z urządzenia we-wy o adresie zawartym w rejestrze C

OUT (n), A

Operation: (n) ← A

Op Code: OUT

Operands: (n), A



Description: The operand n is placed on the bottom half (A0 through A7) of the address bus to select the I/O device at one of 256 possible ports. The contents of the Accumulator (register A) also appear on the top half (A8 through A15) of the address bus at this time. Then the byte contained in the Accumulator is placed on the data bus and written to the selected peripheral device.

M Cycles	T States	4 MHz E.T.
3	11 (4, 3, 4)	2.75

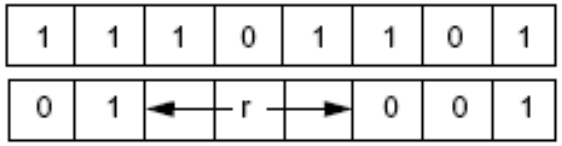
Wyślij zawartość akumulatora A do urządzenia we-wy o adresie n

OUT (C), r

Operation: (C) ← r

Op Code: OUT

Operands: (C), r



Description: The contents of register C are placed on the bottom half (A0 through A7) of the address bus to select the I/O device at one of 256 possible ports. The contents of Register B are placed on the top half (A8 through A15) of the address bus at this time. Then the byte contained in register r is placed on the data bus and written to the selected peripheral device. Register r identifies any of the CPU registers shown in the following table, which also shows the corresponding three-bit r field for each that appears in the assembled object code:

Register	r
B	000
C	001
D	010
E	011
H	100
L	101
A	111

M Cycles	T States	4 MHz E.T.
3	12 (4, 4, 4)	3.00

Wyślij zawartość rejestru r do urządzenia we-wy o adresie zawartym w C

Przesłania blokowe w obszarze pamięci

LDI

Operation: (DE) ← (HL), DE ← DE + 1, HL ← HL + 1, BC ← BC -1

Op Code: LDI

Operands: (SP), HL

1	1	1	0	1	1	0	1	ED
1	0	1	0	0	0	0	0	A0

Description: A byte of data is transferred from the memory location addressed, by the contents of the HL register pair to the memory location addressed by the contents of the DE register pair. Then both these register pairs are incremented and the BC (Byte Counter) register pair is decremented.

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

Condition Bits Affected:

LDIR

Operation: (DE) ← (HL), DE ← DE + 1, HL ← HL + 1, BC F↔ BC -1

Op Code: LDIR

Operands: B8

1	1	1	0	1	1	0	1	ED
1	0	1	1	0	0	0	0	B0

Description: This 2-byte instruction transfers a byte of data from the memory location addressed by the contents of the HL register pair to the memory location addressed by the DE register pair. Both these register pairs are incremented and the BC (Byte Counter) register pair is decremented. If decrementing causes the BC to go to zero, the instruction is terminated. If BC is not zero, the program counter is decremented by two and the instruction is repeated. Interrupts are recognized and two refresh cycles are executed after each data transfer. When BC is set to zero prior to instruction execution, the instruction loops through 64 Kbytes.

For BC ≠ 0:

M Cycles	T States	4 MHz E.T.
5	21 (4, 4, 3, 5, 5)	5.25

For BC = 0:

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

LDD

Operation: (DE) ← (HL), DE ← DE -1, HL ← HL-1, BC ← BC-1

Op Code: LDD

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	0	1	0	0	0	A8

Description: This 2-byte instruction transfers a byte of data from the memory location addressed by the contents of the HL register pair to the memory location addressed by the contents of the DE register pair. Then both of these register pairs including the BC (Byte Counter) register pair are decremented.

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

Condition Bits Affected:

LDDR

Operation: (DE) ← (HL), DE ← D ← 1, HL ← HL-1, BC ← BC-1

Op Code: LDDR

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	1	1	0	0	0	B8

Description: This 2-byte instruction transfers a byte of data from the memory location addressed by the contents of the HL register pair to the memory location addressed by the contents of the DE register pair. Then both of these registers, as well as the BC (Byte Counter), are decremented. If decrementing causes BC to go to zero, the instruction is terminated. If BC is not zero, the program counter is decremented by two and the instruction is repeated. Interrupts are recognized and two refresh cycles execute after each data transfer.

When BC is set to zero, prior to instruction execution, the instruction loops through 64 Kbytes.

For BC ≠ 0:

M Cycles	T States	4 MHz E.T.
5	21 (4, 4, 3, 5, 5)	5.25

For BC = 0:

CPI

Operation: A- (HL), HL ← HL +1, BC ← BC -1

Op Code: CPI

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	0	0	0	0	0	A1

Description: The contents of the memory location addressed by the HL register is compared with the contents of the Accumulator. In case of a true compare, a condition bit is set. Then HL is incremented and the Byte Counter (register pair BC) is decremented.

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

CPIR

Operation: A-(HL), HL ← HL+1, BC ← BC-1

Op Code: CPIR

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	1	0	0	0	1	B1

Description: The contents of the memory location addressed by the HL register pair is compared with the contents of the Accumulator. In case of a true compare, a condition bit is set. HL is incremented and the Byte Counter (register pair BC) is decremented. If decrementing causes BC to go to zero or if A = (HL), the instruction is terminated. If BC is not zero and A ≠ (HL), the program counter is decremented by two and the instruction is repeated. Interrupts are recognized and two refresh cycles are executed after each data transfer.

If BC is set to zero before instruction execution, the instruction loops through 64 Kbytes if no match is found.

For BC ≠ 0 and A ≠ (HL):

M cycles	T States	4 MHz E.T.
5	21 (4, 4, 3, 5, 5)	5.25

For BC = 0 and A = (HL):

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

CPD

Operation: A -(HL), HL ← HL -1, BC ← BC -1

Op Code: CPD

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	0	1	0	0	1	A9

Description: The contents of the memory location addressed by the HL register pair is compared with the contents of the Accumulator. In case of a true compare, a condition bit is set. The HL and Byte Counter (register pair BC) are decremented.

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

Zawartość akumulatora jest porównywana z zawartością komórki o adresie zawartym w HL, w przypadku pozytywnego porównania odpowiedni bit warunkowy jest ustawiany.

CPDR

Operation: A -(HL), HL ← HL -1, BC ← BC -1

Op Code: CPDR

Operands: —

1	1	1	0	1	1	0	1	ED
1	0	1	1	1	0	0	1	B9

Description: The contents of the memory location addressed by the HL register pair is compared with the contents of the Accumulator. In case of a true compare, a condition bit is set. The HL and BC (Byte Counter) register pairs are decremented. If decrementing causes the BC to go to zero or if A = (HL), the instruction is terminated. If BC is not zero and A = (HL), the program counter is decremented by two and the instruction is repeated. Interrupts are recognized and two refresh cycles execute after each data transfer. When BC is set to zero, prior to instruction execution, the instruction loops through 64 Kbytes if no match is found.

For BC ≠ 0 and A ≠ (HL):

M Cycles	T States	4 MHz E.T.
5	21 (4, 4, 3, 5, 5)	5.25

For BC = 0 and A = (HL):

M Cycles	T States	4 MHz E.T.
4	16 (4, 4, 3, 5)	4.00

Porównanie zawartości akumulatora i komórki pamięci zawartej w HL. Adres HL jest dekrementowany. Licznik pętli jest dekrementowany. Gdy A=(HL) lub BC=0000 instrukcja jest przerwana.

Rozkazy arytmetyczne 8-mio bitowe