The New Design of AGC Circuit for the Sinusoidal Oscillator With Wide Oscillation Frequency Range

An Sang Hou and Chin E. Lin

***Abstract*—The typical automatic gain control (AGC) schemes are not suitable for the sinusoidal oscillator with wide oscillation frequency range. To solve this problem, the up–down counter, multiplying digital-to-analog converter, and high-speed comparators are employed to achieve the proposed AGC circuit, which corrects the complex roots of the overall system automatically to the imaginary axis of the complex frequency plane. The negative feedback technique with digital hardware is applied on the loop gain control. No low-pass filter is needed to detect the oscillation amplitude. Thus, this technique is suitable for the sinusoidal oscillator with wide oscillation frequency range. The oscillation frequencies ranging from 7 Hz to 1 MHz are tested with the proposed AGC circuit. The experimental results demonstrate the static characteristics and dynamic responses of the overall system.**

***Index Terms*—Automatic gain control (AGC), digital-to-analog (D/A) converter, sinusoidal oscillator, up-down counter.**

I. Introduction

THE sinusoidal oscillators have many applications in instrumentation, measurement, communication systems, etc. A great variety of active oscillators have been developed for generating sinewaves, most of them based on the use of the conventional operational amplifiers [1], [2], operational transconductance amplifiers [3], and current conveyors [4]–[6]. The oscillation conditions must be satisfied to ensure that the complex roots lie on the imaginary axis of the complex frequency plane. However, parasitic effects or parts mismatch can produce pole displacements large enough to cause the oscillation amplitude to vanish or to increase distortion severely. Therefore, the automatic gain control (AGC) circuit is used to restore the oscillation amplitude to the required level.

The AGC schemes for the sinusoidal oscillator can be found in the literature. The sinusoidal oscillators with digital circuit [7] and multipliers [8] are presented to control the oscillation amplitude. The conditions of oscillation are dependent on the *RC* components relating to the oscillation frequency, and they are violated with the changes of oscillation frequency. Thus, the oscillation amplitudes will vanish or increase distortion severely. Four multipliers and input voltages are employed to implement the AGC circuit for sinusoidal oscillator [9]. The oscillation frequency and amplitude can be tuned with the input voltages. Another AGC scheme [10] employs the ideal half-wave rectifiers and summing circuit to control the oscillation amplitude.

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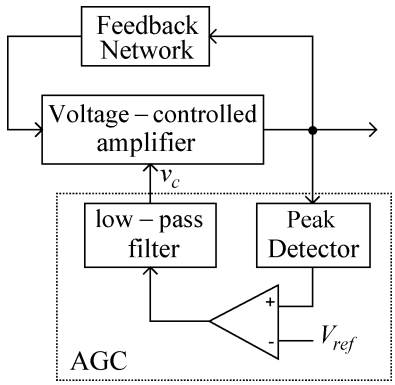

Fig. 1. Scheme of sinusoidal oscillator with typical AGC circuit.

No low-pass filter is needed and thus this scheme can operate over a relatively wide oscillation frequency range. All the mentioned schemes [9], [10] need matched passive-components to keep the condition of oscillation. However, parasitic effects or parts mismatch will cause the oscillation amplitude to vanish or to increase distortion severely. The AGC scheme with average amplitude detection [11], [12] shown in Fig. 1 is used most popularly. The oscillation amplitude is detected and controlled by peak detector, difference amplifier, low-pass filter, and voltage-controlled amplifier. However, the control voltage v_c also varies with the oscillation frequency, and then the oscillation amplitude may vanish or increase distortion severely. Hence, the typical AGC scheme shown in Fig. 1 is not suitable for the sinusoidal oscillator with wide oscillation frequency range.

The sinewave-shaper circuit [13] can change the triangular wave into sinewave signal. This circuit is a practical building block used extensively in function generators and the sinusoidal-type voltage-controlled oscillator (VCO). However, the distortion of the resulting sinewaves may be several percent, which is much worse than the sinewaves produced by the *RC* oscillators. The distortion may induce the phase noise [14], which can be seen from at least two application cases. First, the sinewaves generated from sinewave-shaper circuit are applied to test the frequency responses. Second, the VCO with sinewave-shaper output is employed to implement phase-lock loop. To solve this problem, a new type of AGC circuit is designed to achieve the sinusoidal oscillator with wide oscillation frequency range.

In this paper, the up–down counter, multiplying digital-to-analog (D/A) converter, and high-speed comparators are employed to implement the proposed AGC circuit. No low-pass

TABLE I
KEY FEATURE COMPARISONS OF AGC SCHEMES

Feature \ Schemes	Fianovsky [7]	Fianovsky [8] - [9]	Wojtyna [10]	Average Amp. Detection [11] - [13]	Proposed
Amp. control	Yes	Yes	Yes	Yes	Yes
Matched components	None	Resistors & Capacitors	Resistors	None	None
Auto tuning of osc. condition	No	No	No	Yes	Yes
Wide variation rang of osc.frequency	No	No	No	No	Yes

filter is needed to detect the oscillation amplitude. The overall system exhibits negative feedback effect on the loop gain control. The loop gain of overall system increases with up-count pulses, decreases with down-count pulses, and approaches to unity. As a result, the complex roots of overall system can be automatically corrected to the imaginary axis of the complex frequency plane, the oscillation amplitude can be stabilized, and the oscillation frequency can vary in a wide range. The overall system can also serve as a VCO with little distortion output, if the resistance dominating the oscillation frequency was replaced with a voltage-controlled resistance. The key feature comparisons of AGC schemes are shown in Table I. We can see from Table I that the main superiority of proposed scheme is the applicability of wide variation range of oscillation frequency.

II. CHARACTERISTIC EQUATION

As shown in Fig. 2, the sinusoidal oscillator is realized with the bandpass network and current conveyor, which serves as an amplifier; and its z-terminal is connected to the resistor R_4. We have

$$v_{\rm ref}(s) = \left[\frac{v_\beta(s)}{R_3}\right] \frac{R_4//R_t}{1 + s(R_4//R_t)C_t} \tag{1}$$

where C_t and R_t are transcapacitance and transresistance of AD844, respectively.

The signal $v_{\rm ref}(s)$ serves as the reference input of a 12-bit multiplying D/A converter. The output signal $v_{\rm out}(s)$ is given by

$$v_{\rm out}(s) = v_{\rm ref}(s) \times \frac{\rm dig}{2^{12}} \tag{2}$$

with

$$0 \le {\rm dig} < 2^{12} \tag{3}$$

where the digital value *dig* is fed from the output of 12-bit up–down counter. To prevent the up–down counter from overflow, the maximum value $(\rm FFF)_{16}$ is loaded on the transition of counter value changing from $(\rm FFF)_{16}$ to $(000)_{16}$.

The transfer function of the bandpass network shown in Fig. 2 is

$$\frac{v_\beta(s)}{v_{\rm out}(s)} = \frac{hc\Omega_0 s}{s^2 + c\Omega_0 s + \Omega_0^2} \tag{4}$$

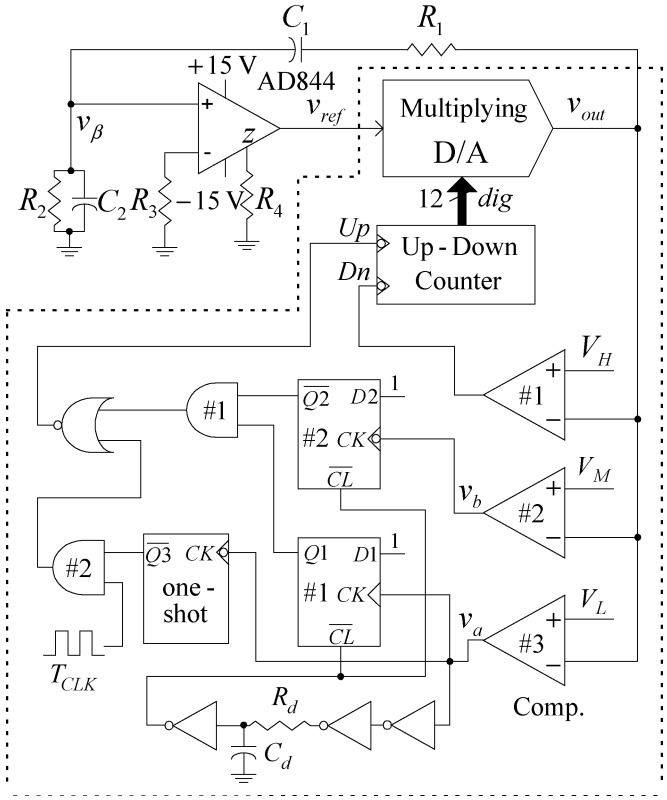

Fig. 2. Sinusoidal oscillator with proposed AGC circuit.

where

$$\Omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{5}$$

$$c = \frac{R_1C_1 + R_2C_2 + R_2C_1}{\sqrt{R_1R_2C_1C_2}} \tag{6}$$

$$h = \frac{R_2C_1}{R_1C_1 + R_2C_2 + R_2C_1}. \tag{7}$$

According to (1), (2), and (4), the characteristic equation of overall system can be derived as

$$s^3 + \left[\frac{1}{\tau} + c\Omega_0\right] s^2 + \Omega_0 \left[\frac{c}{\tau} + \Omega_0 - \frac{chN({\rm dig})}{\tau}\right] s + \frac{\Omega_0^2}{\tau} = 0 \tag{8}$$

with

$$N({\rm dig}) = \frac{(R_4//R_t)}{R_3} \times \frac{\rm dig}{2^{12}}. \tag{9}$$

$$\tau = (R_4//R_t)C_t. \tag{10}$$

From (8) and (9), we can conclude that the characteristic roots can be placed with the digital value dig. According to the Barkhausen criterion, the oscillation frequency and the condition of oscillation can be derived from the loop transfer function as

$$f_{\rm osc} = \frac{\Omega_0}{2\pi\sqrt{1 + c\tau\Omega_0}} \tag{11}$$

and

$$N(\text{dig}) \geq k_m \tag{12}$$

respectively, where

$$k_m = \frac{1}{h}\left[1 + \left(\frac{\tau^2\Omega_0^2}{1 + c\tau\Omega_0}\right)\right]. \tag{13}$$

III. Description of the Proposed AGC Circuit

The schematic diagram of proposed AGC circuit is shown in Fig. 2 inside the dotted line. To generate the trigger pulses rapidly on the transitions that the sinusoidal output voltage $v_{\rm out}(t)$ crosses the reference voltages V_L, V_M, and V_H, the high-speed comparators are implemented with current conveyors, which exhibit slew rate up to 2000 V/μs. The circuit diagram of a high-speed comparator is shown in Fig. 3, where the hysteresis voltage is about 0.045 V to reject the noise disturbance. In order to explain the function of proposed AGC circuit, there are four cases to be discussed.

Case 1) $\max[v_{\rm out}(t)] \leq V_L$.

No pulse is generated from the outputs of comparators #1, #2, and #3 in this case. However, the up-count clocks are generated from the clock source $T_{\rm CLK}$ with $Q1 = 0$, $\overline{Q2} = 1$, and $\overline{Q3} = 1$. Thus, the variable gain N(dig) increases with these up-count clocks. On the condition $N(\text{dig}) > k_m$, the complex roots of (8) lie in the right half of the complex frequency plane and the oscillation grows exponentially.

Case 2) $V_M \geq \max[v_{\rm out}(t)] > V_L$.

In this case, the pulses are generated from comparator #1 and the timing diagram is shown in Fig. 4. The one-shot time is chosen to be greater than the oscillation period of $v_{\rm out}(t)$; thus the clock source $T_{\rm clk}$ is inhibited with $\overline{Q3} = 0$. However, the up-count pulse is generated with $\overline{Q2} = 1$ on the transition of $Q1$ changing from zero to one. The output $Q1$ remains one in the time interval t_d, where t_d is dominated with the time constant R_dC_d shown in Fig. 2. As a result, the variable gain N(dig) increases with up-count pulse in each oscillation cycle of $v_{\rm out}(t)$.

Case 3) $V_H \geq \max[v_{\rm out}(t)] > V_M$.

In this case, the pulses are generated from comparators (#1, #2) and the timing diagram is shown in Fig. 5. The clock source $T_{\rm clk}$ is also inhibited with $\overline{Q3} = 0$. The output of AND-gate #1 is zero, due to the fact that the output ($\overline{Q2}$, $Q1$) is not equal to (1, 1) at the same time. As a result, no count pulse is generated from *Up* input and *Dn* input, the variable gain N(dig) hold on present state.

Case 4) $\max[v_{\rm out}(t)] > V_H$.

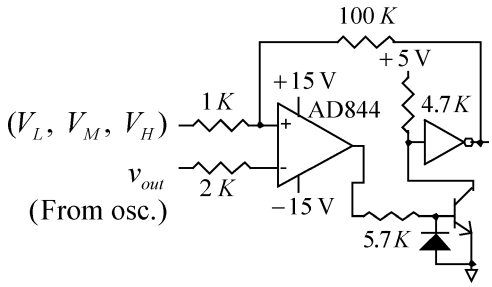

Fig. 3. Circuit diagram of high-speed comparator.

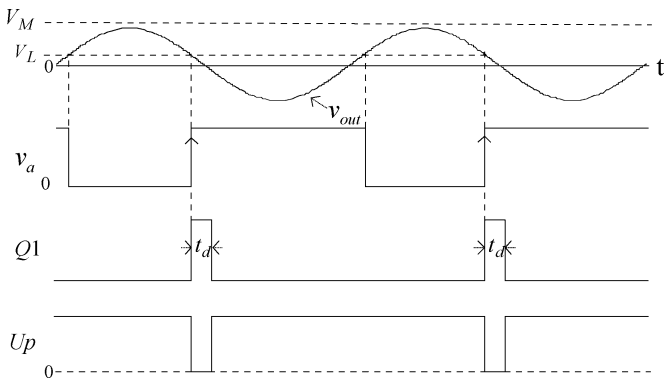

Fig. 4. Timing diagram of the case $V_M > \max[v_{\rm out}(t)] > V_L$.

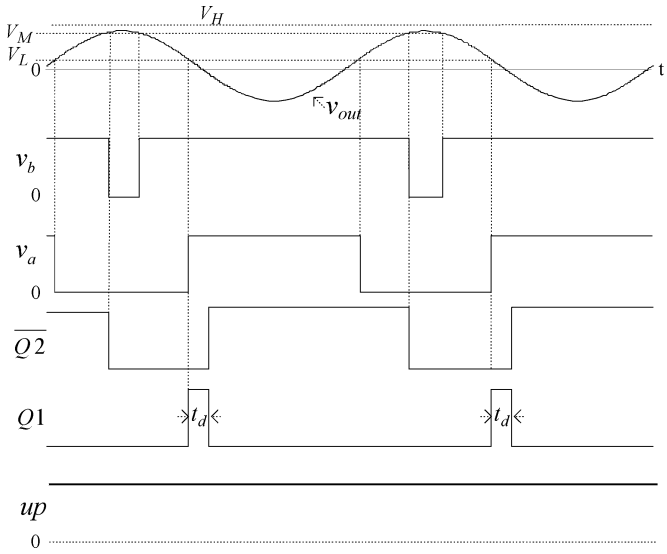

Fig. 5. Timing diagram of the case $V_H \geq \max[v_{\rm out}(t)] > V_M$.

As discussed in Case 3), the pulses are generated from comparators (#1, #2) and then no up-count pulse is generated from *Up*-input. However, the down-count pulse is generated while the oscillation output $v_{\rm out}(t)$ is below the reference voltage V_H and crosses it. Thus, the variable gain N(dig) decreases with down-count pulse in each oscillation cycle of $v_{\rm out}(t)$. As long as $N(\text{dig}) > k_m$, the peak voltage $\max[v_{\rm out}(t)]$ is equal to the positive saturation voltage $+V_{\rm sat}$ in steady state. The down-count pulses disappear immediately after $N(\text{dig}) < k_m$ and $\max[v_{\rm out}(t)] \leq V_H$. The constraint $+V_{\rm sat} > V_H$ must be made to prevent the oscillation output $v_{\rm out}(t)$ from saturation distortion in steady state, where $+V_{\rm sat}$ is the saturation voltage of the sinusoidal oscillator.

It is interesting to note that the overall system exhibits the effect of negative feedback on loop gain control. As a result, the conditions

$$V_H \geq \max\left[v_{\text{out}}(t)\right] > V_M \tag{14}$$

and

$$N(\text{dig}_{ss}) \rightarrow k_m \tag{15}$$

remain true in steady state, where dig_{ss} is the 12-bit D/A input value in steady state. Thus, the sinewave with little distortion can be generated from the output $v_{\text{out}}(t)$ according to (8) and (15), where the peak voltage $\max[v_{\text{out}}(t)]$ is constrained by (14).

To ensure that the complex roots of (8) are placed on the right half of complex frequency plane initially and thus the oscillation can be self-starting, the following:

$$N\left[(\text{FFF})_{16}\right] > k_m \tag{16}$$

should be satisfied, where $(\text{FFF})_{16}$ is the maximum value of 12-bit D/A input dig and k_m is defined in (14). The variable gain $N(\text{dig})$ is tuned automatically with the proposed AGC circuit so that (16) remains true. As a result, the condition of oscillation shown in (12) can be rewritten with (5)–(7), (9), (13), and (16). That is

$$\frac{(R_4//R_t)}{R_3} > \left(\frac{R_1C_1 + R_2C_2 + R_2C_1}{R_2C_1}\right) \times \left[1 + \frac{\tau^2}{R_1R_2C_1C_2(R_1C_1 + R_2C_2 + R_2C_1)\tau}\right] \tag{17}$$

where τ is defined in (10) and the resistors (R_1, R_2, R_3, R_4) and capacitors (C_1, C_2) are depicted in Fig. 2.

IV. Truncation Error

Due to the function of the proposed AGC circuit, the complex roots of (8) can be placed on the imaginary axis of complex frequency plane in steady state. Thus, the positive real number r_0 can be found so that the variable gain $N(\text{dig})$ is equal to k_m, that is

$$\frac{(R_4//R_t)}{R_3} \times \frac{r_0}{2^{12}} = k_m \tag{18}$$

with

$$r_0 = \text{dig}_{ss} + \varepsilon \tag{19}$$

where ε is the truncation error of r_0 into the digital value dig_{ss}. The range of truncation error ε is

$$0 < \varepsilon < 1. \tag{20}$$

According to (9), (18), and (19), the variable gain in steady state is given by

$$N(\text{dig}_{ss}) = k_m - \frac{(R_4//R_t)}{R_3} \times \frac{\varepsilon}{2^{12}}. \tag{21}$$

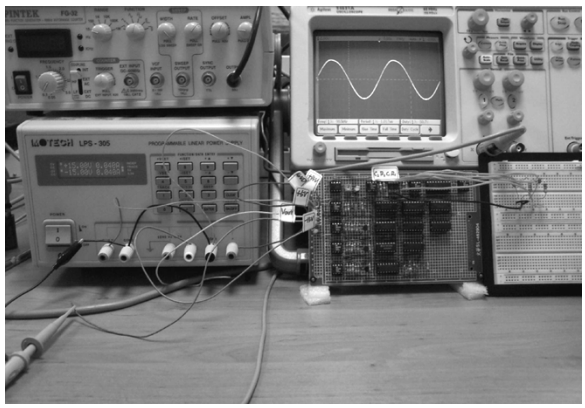

Fig. 6. Overall circuit and test equipment.

The complex roots of overall system can be derived from (6)–(8) and (21) with dig= dig_{ss}. That is

$$(s_1, s_2) = \Big[2\pi f_{\text{osc}}(-\varepsilon\Delta + \sqrt{1-\varepsilon^2\Delta^2}\,j), \; 2\pi f_{\text{osc}}(-\varepsilon\Delta - \sqrt{1-\varepsilon^2\Delta^2}\,j)\Big] \tag{22}$$

where

$$\Delta = \frac{(R_4//R_t)}{R_3} \times \frac{R_2C_1}{2^{13}\sqrt{R_1R_2C_1C_2}} \tag{23}$$

and f_{osc} is defined in (11). Therefore, the oscillation frequency is given by

$$f'_{\text{osc}} = f_{\text{osc}}\sqrt{1-\varepsilon^2\Delta^2}. \tag{24}$$

To measure the frequency variation caused by the truncation error ε, we define

$$\delta_f = \left[\frac{f_{\text{osc}} - f'_{\text{osc}}}{f_{\text{osc}}}\right] \times 100\% = (1 - \sqrt{1-\varepsilon^2\Delta^2}) \times 100\% \tag{25}$$

where δ_f is the variation of oscillation frequency as related to the nominal frequency f_{osc}. From (25) we can see that the variation of oscillation frequency caused by the truncation error ε is very small.

In steady state, the output $v_{\text{out}}(t)$ depicted in Fig. 2 will take the form

$$v_{\text{out}}(t) = V_A e^{-2\pi\varepsilon\Delta f_{\text{osc}}t}\sin(2\pi\sqrt{1-\varepsilon\Delta}f_{\text{osc}}t + \phi_m) \tag{26}$$

where ϕ_m is dependent on the initial condition. Due to the function of the proposed AGC circuit, we have

$$V_M < V_A e^{-2\pi\varepsilon\Delta f_{\text{osc}}t} \leq V_H. \tag{27}$$

The reference voltage V_M is chosen to be very near to the reference voltage V_H. Thus, the oscillation amplitude of $v_{\text{out}}(t)$ remains almost constant.

V. Laboratory Results

Based on the discussion of proposed AGC circuit, the static characteristics and dynamic responses are demonstrated in this section. Fig. 6 shows the overall circuit and test equipment,

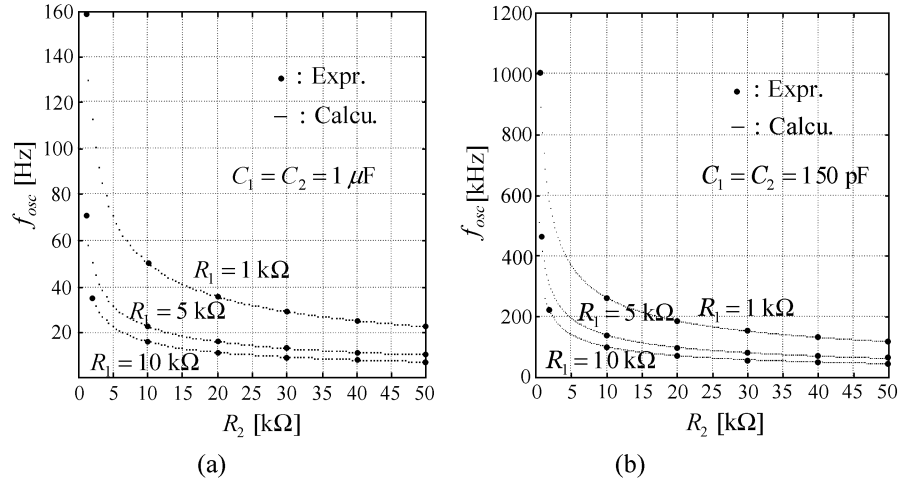

Fig. 7. Test results of $f_{\rm osc}$ versus R_2 with (a) $C_1 = C_2 = 1\ \mu$F and (b) $C_1 = C_2 = 150$ pF, respectively, for R_1 fixed to be 1, 5, and 10 kΩ.

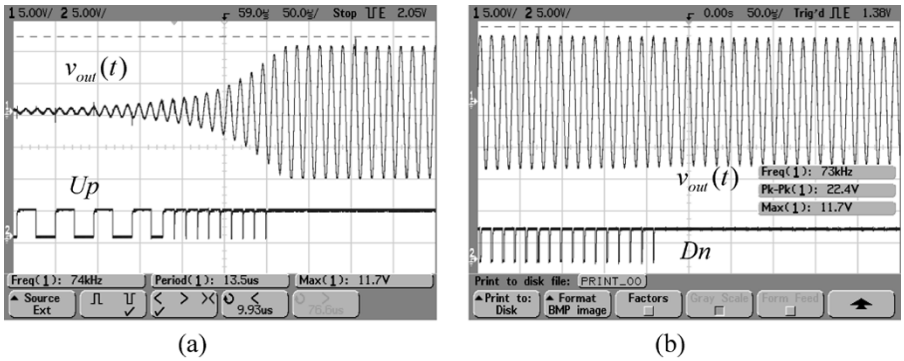

Fig. 8. Experimental results of output responses with (a) up-count and (b) down-count pulses.

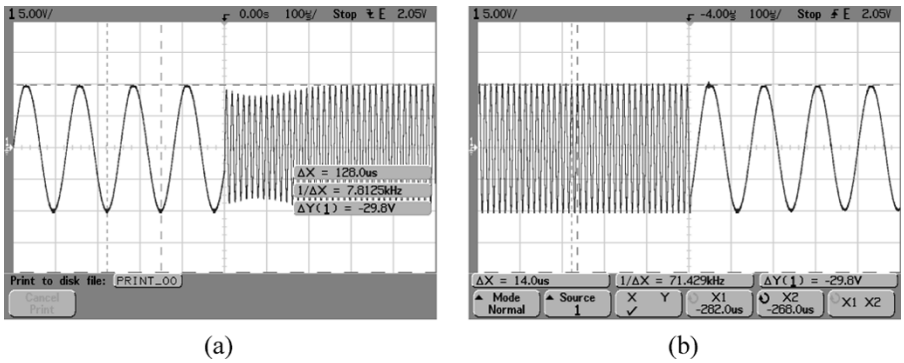

Fig. 9. Sinusoidal output responses to a step frequency change from (a) 7.8 to 71.4 kHz and (b) vice versa.

which includes power supply, oscilloscope, and function generator. The type of oscilloscope is AGILENT 54 621A. The waveforms and measurement results displayed in the screen of oscilloscope can be converted into a bitmap file, which can be saved to a floppy disk. The resistors (R_2, R_1) and capacitors (C_2, C_1) are fed from the breadboard, so that they can be changed flexibly. The step-change resistances of (R_2, R_1) can be done with function generator and the analog switches DG201. The test results of $f_{\rm osc}$ versus the different choices of (R_2, R_1, C_2, C_1) are shown in Fig. 7. The time responses of oscillator output $v_{\rm out}$ are demonstrated in Figs. 8 and 9.

The sinusoidal oscillator employed in this paper is implemented with current conveyor, which exhibits little distortion output [15]. The parts numbers of the 12-bit multiplying D/A converter and current conveyor are AD7541 and AD844, respectively. In Fig. 2, the time constant of one-shot is chosen to be 0.5 s. The supply voltages of ±15 V are employed in the sinusoidal oscillator and proposed AGC circuit. The reference voltages (V_H, V_M, V_L) are chosen to be (10 V, 9.6 V, 2.1 V), respectively, where V_H is less than the saturation voltage of the sinusoidal oscillator. The voltage gain $(R_4//R_t)/R_3$ is 9.97 with $R_4 = 10$ kΩ, $R_t = 3$ MΩ [16], and $R_3 = 1$ kΩ.

In order to verify the oscillation frequency and condition of oscillation shown in (11) and (17), respectively, the resistance R_2 is tested and the oscillation frequency is recorded with respect to the different choices of R_1, C_1 and C_2. Fig. 7 shows the allowable range of R_2 with $R_4/R_3 = 9.97$ so that the oscillation can be self-starting and the oscillation frequency $f_{\rm osc}$ sustains with little distortion in steady state. In Fig. 7(a) and (b), the test results of $f_{\rm osc}$ versus R_2 are depicted with $C_1 = C_2 = 1\ \mu$F and $C_1 = C_2 = 150$ pF, respectively, for R_1 fixed to be 1, 5, and 10 kΩ. The test range of oscillation frequency $f_{\rm osc}$ is from 7 Hz to 1 MHz and the frequency of clock source $T_{\rm CLK}$ is chosen to be 20 kHz.

It is seen from Fig. 7 that the allowable oscillation frequency is wide and the experimental results match with the predictions of (11) and (17). In a similar way, the test results of $f_{\rm osc}$ versus R_1, C_1 and C_2 with respect to the different choices of (R_2, C_1, C_2), (R_1, R_2, C_2) and (R_1, R_2, C_2), respectively, can be obtained.

In Fig. 8, the sinusoidal oscillator with oscillation frequency equal to 73 kHz is employed to demonstrate the dynamic performances of the proposed AGC circuit. The up-count clocks are fed from the clock source $T_{\rm clk}$ while $\max[v_{\rm out}(t)] \leq 2.1$ V. As depicted in Fig. 8(a), the clock source $T_{\rm clk}$ is inhibited on the transition from $\max[v_{\rm out}(t)] \leq 2.1$ V to $\max[v_{\rm out}(t)] > 2.1$ V and the up-count pulse is generated from AND-gate 1 in each oscillation cycle of $v_{\rm out}(t)$. The oscillation keeps growing and the up-count pulses are inhibited on the condition $\max[v_{\rm out}(t)] > 9.6$ V. As depicted in Fig. 8(b), the down-count pulses are generated from the output of comparator 1 shown in Fig. 2, while $\max[v_{\rm out}(t)] > 10$ V. Thus, the loop gain $N(\text{dig})h$ decreases with the down-count pulses. The peak voltage $\max[v_{\rm out}(t)]$ is equal to the positive saturation voltage while the condition $N(\text{dig}) > k_m$ remains true. The down-count pulses disappear immediately after $N(\text{dig}) < k_m$ and $\max[v_{\rm out}(t)] \leq 10$. In steady state, the conditions $N(\text{dig}) \rightarrow k_m$ and 9.6 V $< \max[v_{\rm out}(t)] \leq 10$ V remain true, where 9.6 and 10 V are the reference voltages V_M and V_H, respectively.

In order to demonstrate the validity of the proposed AGC circuit with wide oscillation frequency range, Fig. 9 shows the experimental results to illustrate the output response to a sudden change of oscillation frequency. The resistances (R_1, R_2) on the condition $C_1 = C_2 = 1$ nF are changed with analog switches from (21 kΩ, 21 kΩ) to (2.2 kΩ, 2.2 kΩ) and vice versa; the corresponding oscillation frequency as depicted in Fig. 9 changes from 7.8 to 71.4 kHz and vice versa. We can see from Fig. 9(a) and (b) that the sinusoidal oscillations sustain with little distortion in steady state.

VI. Conclusion

A new AGC circuit design for sinusoidal oscillator has been presented in this paper. Furthermore, no matched component is needed to implement it and the sinusoidal oscillator. No low-pass filter is needed to detect the oscillation amplitude. Without any modification of the AGC circuit, the applicability of the wide oscillation frequency variation of the sinusoidal oscillator has been verified successfully in the range from 7 Hz to 1 MHz. It is an importance issue for the design of the sinusoidal oscillator.

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