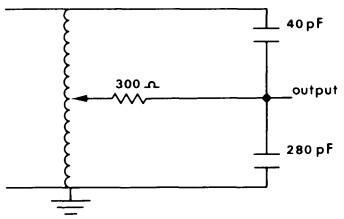


Fig. 3. Equivalent circuit of the ratio transformer, derived from phase-error measurements.

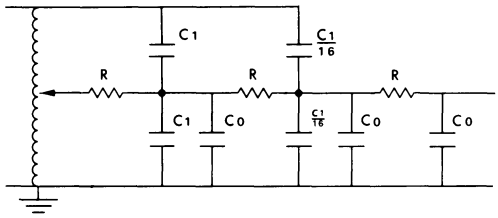


Fig. 4. A more detailed equivalent circuit from which Fig. 3 may be obtained using component values given in the text.

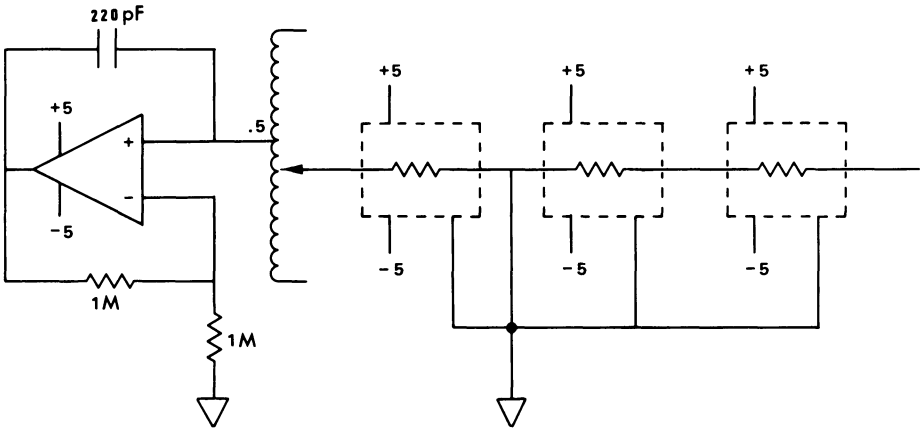


Fig. 5. A quadrature compensation circuit in which the digital power supply common is connected to the second-stage output.

CMOS switches. $C_0$ = 120 pF is the output capacitance to ground of the switches, and $R$ = 100 Ω, their "on" resistance.

The major quadrature error arises from the lag caused by the equivalent 280-pF capacitance. This can be canceled by introducing a phase lead proportional to the output signal in an operational amplifier drive circuit usually required to prevent loading the transformer. Alternatively, a circuit as shown in Fig. 5 can be used to cancel practically all quadrature signals. This circuit removes the effects of $C_0$ by connecting the digital power supply common to the second-stage output voltage. The phase shift due to $C_1$ in the second stage is zero at the 0.5 setting of the transformer. At a setting different from 0.5, a quadrature compensation is required. The FET amplifier amplifies this difference with a gain of one-half and supplies the compensating signal through a capacitor approximately equal to twice the value of $C_1$ or 220 pF (Fig. 5). This arrangement necessitates a floating digital power supply and optical isolators to interface with the computer.

## Conclusion

The combination of multistage design and solid-state switches offers a very cost effective means of realizing accurate, stable, and programmable ratio transformers particularly suitable for low-frequency applications. Such a voltage ratio device is currently used in an automatic thermometer bridge operating at 30 Hz.

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## A Wien-Bridge Oscillator with High-Amplitude Stability

P. W. VAN DER WALT, MEMBER, IEEE

***Abstract*—A FET-stabilized Wien-bridge oscillator, capable of maintaining an output voltage of 5 V to an accuracy of 0.02 percent with total harmonic distortion 0.01 percent is described. A linear model is presented for the amplitude-stabilizing control loop from which useful design relationships are developed.**

Manuscript received February 26, 1980; revised June 16, 1981.

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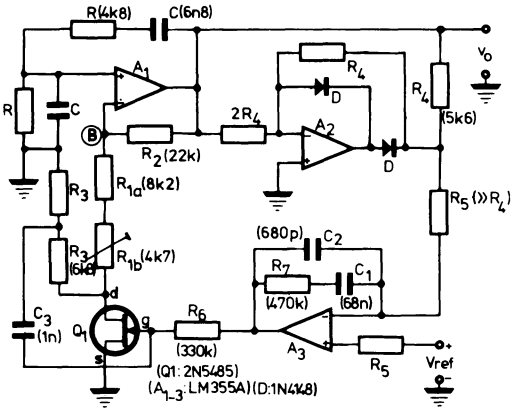


Fig. 1. FET-stabilized Wien-bridge oscillator.

## I. Introduction

The FET-stabilized Wien-bridge oscillator is well known [1]–[3]. A low-distortion version, which was developed as a signal source in a precision capacitance measuring bridge is described.

The oscillator was specified to oscillate at a nominal frequency of 5 kHz, with the output voltage maintained at 5000 ± 1 mV rms over the temperature range 0 to 40°C. The total harmonic distortion of the oscillator was measured as 0.01 percent.

A linear model is developed for the control loop, from which the small-signal behavior of the control loop can be predicted. This leads to design equations for the amplitude-stabilizing loop.

## II. Circuit Diagram

The circuit diagram of the oscillator with its amplitude-stabilizing loop is shown in Fig. 1.

The output voltage of the Wien-bridge oscillator is fed to a full-wave rectifier. The difference between the output voltage of the rectifier and the reference voltage $V_{\text{ref}}$ is integrated and filtered to obtain a dc control voltage at the gate of the FET, which controls the ac drain–source resistance of the FET in such a way that the output voltage of the oscillator is maintained at a constant amplitude. The ac characteristic of the FET is linearized by superimposing one half of the drain–source voltage on the gate–source control voltage.

The oscillator oscillates at a frequency

$$f = \frac{1}{2\pi RC}. \tag{1}$$

In a stable loop, the integrator forces the difference between $V_{\text{ref}}$ and the mean value of the rectified output voltage of the oscillator to zero, thus maintaining the amplitude of oscillation at a precise value.

With $V_o$ denoting the peak value of the output voltage, and assuming that the components are ideal, the mean value of the output voltage of the rectifier will be $V_o/\pi$, which leads to the conclusion that

$$V_o = \pi V_{\text{ref}}. \tag{2}$$

## III. Output-Voltage Drift

As any static error due to component tolerances can be adjusted to zero by adjusting $V_{\text{ref}}$, the only cause for changes in output amplitude will be temperature drift. With the assumption that the resistors in the rectifier circuit will track each other with changes in temperature (as will be the case if thick- or thin-film resistors on a common substrate are used), the only significant sources of amplitude error are the input-offset voltages $V_{ioj}$ and input-offset currents $I_{ioj}$ of the operational amplifiers $A_j$ in Fig. 1.

If the effects of these voltages and currents are referred to the output of the rectifier, and $I_{io1}$ and $I_{io2}$ are disregarded because their effect is negligible if FET-input amplifiers are used, it is found that, under stationary conditions

$$\Delta V_o = \pi\left(\frac{3}{2}V_{io1} + V_{io2} + V_{io3} + I_{io3}R_5\right) \tag{3}$$

where $\Delta V_o$ is the change in peak output voltage from the nominal value.

If LM355A operational amplifiers are used throughout, and if the worst case condition, where all offset drifts add, is assumed, the temperature drift of $V_o$ is calculated as 55 $\mu$V(peak)/°C, resulting in a maximum drift of ±0.78 mV rms over the temperature range 20 ± 20°C.

## IV. Feedback-Loop Dynamics

The small-signal response of the amplitude-stabilizing loop (i.e., the amplitude response of the oscillator for small disturbances in the control loop) can be analyzed once a suitable linear model for the oscillator has been obtained.

If all the components are ideal, the oscillator will oscillate with a stable amplitude if $R_B = \frac{1}{2}R_2 = R_{B0}$, where $R_B$ is the total resistance between node $B$ and ground in Fig. 1. With $R_B$ perturbed to a value $R_B = R_{B0} + \Delta R_B$, the poles of the Wien-bridge oscillator may be determined as the roots of the equation

$$s^2 + \frac{2\Delta R_B}{R_{B0}RC}s + \frac{1}{R^2C^2} = 0. \tag{4}$$

If now $R_B = R_{B0}$ up to time $t = 0$, the oscillator is oscillating at a stable output level of $V_{o0}$ up to this time, and $R_B$ is suddenly changed to $R_{B0} + \Delta R_B$, the amplitude of oscillation will change exponentially after time $t = 0$. The amplitude of oscillation as a function of time for $t > 0$ is determined as

$$V_o(t) \simeq V_{o0}\left(1 - \frac{2\Delta R_B}{3R_{B0}}\right)\exp\left(\frac{-\Delta R_B}{R_{B0}RC}t\right) \tag{5}$$

by circuit analysis.

For small excursions around the nominal operating point, (5) may be approximated as

$$V_o(t) \simeq V_{o0}\left(1 - \frac{2\Delta R_B}{3R_{B0}}\right)\left(1 - \frac{\Delta R_B}{R_{B0}RC}t\right). \tag{6}$$

The response (6) is identical to the response of a system with transfer function

$$G = -\frac{V_{o0}\left(1 + \dfrac{2sCR}{3}\right)}{sCR} \tag{7}$$

which is driven by an input step waveform of magnitude $\Delta R_B/R_{B0}$.

In the feedback loop shown in Fig. 1, the zero of the transfer function (7) can be ignored, because it has no significant effect on the dynamic response of the system.

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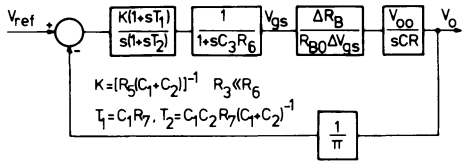


Fig. 2. Block diagram of the amplitude-stabilizing loop.

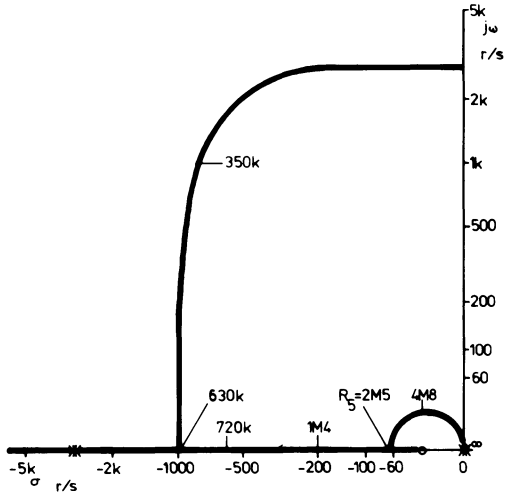


Fig. 3. Root-locus plot for the control loop with element values shown in Fig. 1 and $1/R_5$ as gain variable.

This model of the oscillator leads to the block diagram shown in Fig. 1. The FET is also modeled as a linear element. Because the ac drain-source voltage is small, the FET may be regarded as a linear resistor between the drain and source terminals. Because small-signal conditions are also assumed in the control loop itself, the gate-source voltage to drain-source ac resistance transfer characteristic may also be considered to be linear with transfer function

$$H = \frac{\Delta R_B}{R_{B0}\Delta V_{gs}}\bigg|_{V_{gs}=0}. \tag{8}$$

The operating point $V_{gs} = 0$ ensures that the drain-source ac resistance will be small, thus ensuring a small ac voltage across the FET.

The design considerations for the control loop depend on whether the oscillator is designed for low distortion or fast dynamic response. In the case of low distortion, care must be taken to ensure that the harmonic components in the output signal of the rectifier (the first of which lies at twice the oscillator frequency) are highly attenuated at the gate of the FET. This is ensured if the time constants $T_2$ and $C_3R_6$ (Fig. 2) are approximately ten times larger than the product $RC$, and if $T_1$, which serves to stabilize the loop, is larger than $T_2$ by a factor of 50 or more.

The element values shown in Fig. 1 were chosen for low distortion. Resistor $R_{1b}$ is made adjustable to compensate for FET and component tolerances; it should be adjusted so that $V_{gs} \simeq 0$. A root-locus plot for the control loop with the element values in Fig. 1 and $1/R_5$ as gain variable is shown in Fig. 3 on nonlinear scales. From the plot, a value of 820 kΩ for $R_5$ would ensure a good dynamic response for the loop.

The circuit may be scaled to operate at other frequencies by scaling all capacitors by the same factor.

## V. Conclusion

A low-distortion version of the FET-stabilized Wien-bridge oscillator having high amplitude stability has been described. A model has been presented for the amplitude-stabilizing control loop which leads to a straightforward design procedure. The model can be adapted to oscillators other than the Wien bridge by determining the response of the oscillator to a perturbation of the stabilizing elements.

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# An Autoranging Voltmeter Circuit Without Range Resistors

L. Y. HUNG

***Abstract*—An autoranging circuit for digital voltmeter without range resistors is presented. The circuit uses a microprocessor-based time-averaging technique. This technique can achieve an accuracy comparable to a 4½ digit DVM in 5-decade range. An autozero and autopolarity circuit is also presented.**

## Introduction

There are different techniques [3], [4] available today for designing a autoranging digital voltmeter DVM. All of them rely on one set of accurate voltage dividers which can be selected by electronically controlled switches. This short paper investigates a technique by which these switches and the voltage dividers can be eliminated without sacrificing the dynamic range and the relative accuracy of the meter. The technique is based on the computational capability of a microprocessor. Since today's semiconductor technology has narrowed the price gap between a microprocessor and an accurate voltage divider network, this implementation is also economically feasible for general-purpose DVM application.

## Principle of Operation

Fig. 1 illustrates the basic principle of this circuit. A negative input voltage $V_x$ is applied to the integrator $A_1$, and the capacitor $C_1$ is charged up until $V_c$, the output voltage of $A_1$, reaches a bias voltage $V_B$. Then the comparator $A_2$ will trigger a one-shot multivibrator to generate a pulse of fixed width $T_p$, which closes the switch $SW_a$. Since $V_s/R_s$ is greater than $V_x/R_i$, $V_c$ will slope downward during this interval. When $T_p$ has elapsed, the $SW_a$ is opened, and the process repeats. The output pulses from the multivibrator are also fed to a counter for frequency measurement. In steady-state condition, the charge-balancing equation is

$$T_p\left(\frac{V_s}{R_s} - \frac{V_x}{R_i}\right) = T_i\frac{V_x}{R_i} \tag{1}$$

where $T_i$ is the input voltage integrating time. Equation (1) can be rearranged as

$$\frac{1}{T} = \frac{1}{T_p}\frac{V_x}{V_s}\frac{R_s}{R_i} \tag{2}$$

Manuscript received October 20, 1980; revised May 27, 1981.

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