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Low Cost Ultra-Pure Sine Wave Generation with Self Calibration

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Abstract

As data acquisition systems' performance continues to increase, so does the need for a test and characterization solution to have an input test signal with purity that exceeds what is currently available in state of the art instruments. This paper presents a new method for generating ultra-pure sine wave that can be used in such applications. The pure sine wave is generated by readily available DACs with distortions that could be thousands time worse than the required system purity. Readily available ADC with similar purity as the DAC is used to measure the distortions generated by the DAC. Innovative algorithm is used to iteratively remove distortions present in the generated sine wave. Simulation results verified the proposed method by generating a -140dB ultra-pure sine wave using two DACs and an ADC with -85dB THD. A test board has been designed and measurement results demonstrated that generated sine wave has the high purity that is capable of testing an ADC with -120dB THD accurately.

Keywords - Digital-to-Analog Converter; nonlinear source; signal purity; Analog-to-Digital Converter; spectral testing.

1. Introduction

Data Converters play a crucial rule in electronics field as they bridge the analog world to the digital domain and vice-versa in modern Integrated Circuits (ICs). Over the last decades, significant progress has been achieved in designing high precision data converters [1]. Nowadays, 16 bit Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are commonly used in IC design. Applications such as precision measurement, seismic signal conditioning and precision analog microcontrollers push the designer to achieve even higher performance of data converters [2]. In order to characterize such sophisticated devices, high end Automatic Test Equipment (ATE) are now widely used in industrial and consumer products. Among many test mechanisms to quantify the performance of data converters, spectral testing is one of the widely used mechanisms. Spectral testing involves testing the data converter for dynamic specifications that are key to determining its performance. Both IEEE standard 1241 [3] and IEEE standard 1057 [4] list several requirements in order to accurately perform spectral testing. One of the requirements is that the input signal for the ADC under test needs to be 3 to 4 bits more pure than the ADC. This requirement becomes more challenging when the resolution of the ADCs becomes higher.

In the literature, many researchers have proposed their methods to generate high purity, low distortion sine waves. In [9], a high purity sine wave was generated with an Arbitrary Waveform Generator (AWG), by removing unwanted harmonics and spurs, and applying correct signal, a high purity sine wave can be generated. Later, A. Maeda proposed a method to generate very low distortion, high frequency sine wave [10]. By applying calibration signals that are reverse vectors to the harmonics at output to cancel out distortions, a very low distortion sine wave can be created. In [11], by changing AWG program to suppressed 3rd order harmonics and filter out spurious components, a low distortion sine wave can be generated. In [12], a method is proposed, which generates an ultra-pure sine wave from outputs of a phase shift oscillator by cancelling the harmonics using weighing and summing of the outputs. THD smaller than -100dBc was reported. In [13], Elsayed, et al. proposed an architectural solution for designing low THD oscillators, with a digital harmonic-cancellation-block and passive filter, THD of –73dB was shown at 10MHz. All of these method have demonstrated their effectiveness via measurements and they can be easily implemented in standard labs with low cost. However, the generated sine waves purity, although showed great improvement, are still not sufficient to meet the stringent test requirement nowadays.

In industry, several high performance equipments are widely used nowadays to test high resolution ADCs. The latest Audio Precision APx series signal generator such as APx 555 is capable of generating very low distortion sinusoidal signal with purity levels of -120dB [5]. This demonstrated its high performance as an analog source and found its applications in various high precision test environments. Data Converter Test Module (DCTM) instrument also provides capabilities to meet the requirements of high precision data converter test. It can produce -120dB purity level of low distortion sine wave by utilizing stringent test diagnostics and calibrations [6].

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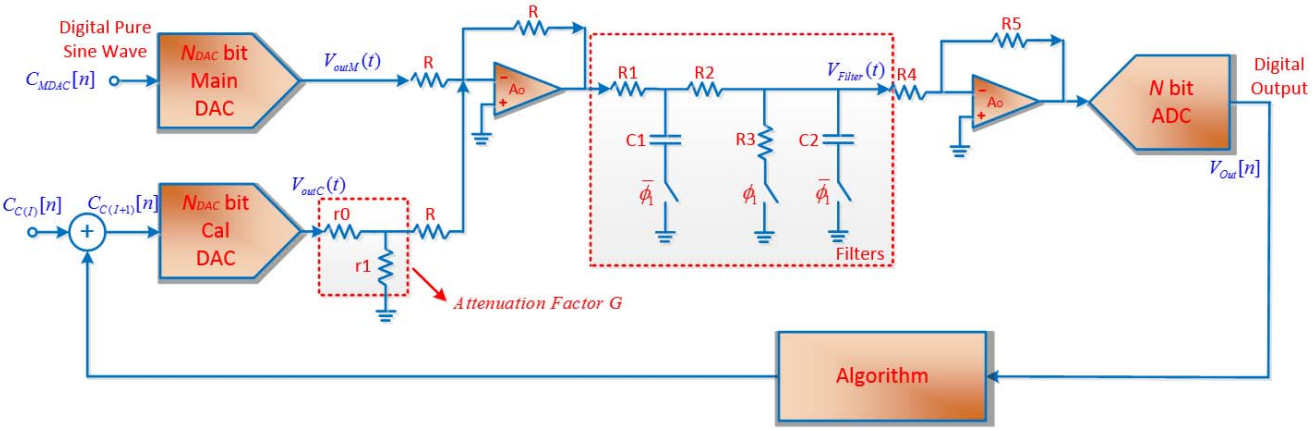

Figure 1: Test setup diagram of proposed method

However, such purity level is achieved either through sophisticated circuitry design, or complicated calibration, which requires lots of design efforts and careful design considerations. These test equipments, though accurate, are large and extremely costly, which limits their practical usage in standards labs.

Although costly, such signal generator may not meet the stringent requirements as the performance of the device under test becomes higher. For example, an 18 bit ADC would require at least -130dB purity of the input signal. In addition, when the resolution becomes even higher, the signal generation equipment may not be available for such high purity. In that case, the ADC output spectrum will no longer contain just ADC nonlinearity, but also contains nonlinearity from the input. The ADC's specifications such as Total Harmonic Distortion (THD) and Spurious Free Dynamic Range (SFDR) cannot be accurately obtained from the output spectrum. Therefore, a method is needed to generate such high purity sinusoidal signal at low cost. In this paper, we propose a signal generator that can provide ultra-pure sine wave through novel iterative algorithm with readily available devices. The method is computationally efficient with self-calibration and readily implemented to applications that require high purity sine waves.

The rest of the paper is arranged as follows: Section II describes the proposed method for generating ultra-pure sine wave. Section III presents the simulation results in MATLAB. Section IV validates the proposed method by measurement results and Section V concludes the paper.

2. Ultra-pure Sine Wave Generation

The proposed setup is shown in Figure 1: two DACs, the Main DAC and the Calibration (Cal) DAC are summed together to get the buffered output. The Cal DAC output is attenuated by a simple RR attenuator, with an attenuation factor of $G = r0/r1$, whose role is discussed later. Then two different filters: RR attenuator and RC filter are connected after the summed buffer. The output of these filters will be the ADC inputs. When one filter is connected, the other filter is switched off, so the input of both filters would be the same, but ADC will have two different inputs that are spectrally related based on the transfer functions of both filters. The two ADC outputs are acquired for further processing.

2.1 Signal Derivation

At first iteration, the Main DAC generates its nonlinear output signal, which is later used as ADC's input signal. The Cal DAC is turned off so $C_{FDAC(I)} = 0$. The Main DAC input codes $C_{MDAC}(t)$ are given by:

$$C_{MDAC}(t) = round\left(\left(\frac{V_{RDAC}}{2} + |A|\cos(\omega_o t + \phi)\right) \times 2^{N_{DAC}}\right) \quad (1)$$

Where; $t \in [iT_{sDAC}, (i+1)T_{sDAC})$, $i = 0,1,2...M_{DAC} - 1$, T_{SDAC} stands for DAC sampling period; M_{DAC} is the data record length of DAC input codes; $|A| \le \frac{V_{RDAC}}{2}$; the DAC output range is $[0\ V_{RDAC}]$ and has resolution of N_{DAC} bit; ϕ is the initial phase of the input signal, and $f_{sig} = \frac{\omega_o}{2\pi}$ is the input frequency of the input signal.

The ideal DAC analog output signal is given by:

$$V_{out\_ideal}(t) = \frac{C_{in}(t)}{2^{N_{DAC}}} = \frac{V_{RDAC}}{2} + |A|\cos(\omega_o t + \phi) + Q_{DAC} \quad (2)$$

Where the quantization error of the DAC is given by:

$$Q_{DAC} = round\left(\left(\frac{V_{RDAC}}{2} + |A|\cos(\omega_o t + \phi)\right) \times 2^{N_{DAC}}\right) - \frac{V_{RDAC}}{2} - |A|\cos(\omega_o t + \phi)) \quad (3)$$

In reality, noise and nonlinearities will be added to the output of the DAC. Since the algorithm cannot distinguish the nonlinearities from the Main DAC and its buffer, their noise and nonlinearities are lumped together for algorithm estimation and calibration. Therefore, combined with Main DAC and the buffer at output, the output signal is given by:

$$V_{outM}(t) = \frac{V_{RDAC}}{2} + |A|\cos(\omega_o t + \phi) + Q_{DAC} + \sum_{k=2}^{+\infty} A_k \cos(k\omega_o t + \phi_k) + w(t) \quad (4)$$

Where *w(t)* is the combined noise of Main DAC and the buffer. It can also be rewritten into exponential form:

$$V_{Buffer}(t) = D_0 + \sum_{k=\pm 1}^{\pm H} |D_k| e^{j\cdot k\omega_o t} e^{j\cdot\phi_k} + W_{MDAC}(t) \quad (5)$$

Where $D_0 = \frac{V_{RDAC}}{2}$, $|D_1| = |D_{-1}| = \frac{|A|}{2}$, $|D_k| = |D_{-k}| = \frac{|A_k|}{2}$, ϕ_1, ϕ_k are fundamental's and k[th] harmonics phase, respectively. $W_{MDAC}(t)$ is the total noise including quantization noise and output noise of the Main DAC and buffer. $k = 1, 2, ...H$, and first H harmonics are considered for analysis, assuming that higher order harmonics have negligible power.

After the buffer, two filters are connected between Main DAC and the ADC. The filter outputs are given by:

$$V_{Filter1}(t) = D + \sum_{k=\pm 1}^{\pm H} |D_k H_1(jk\omega_o)| e^{j\cdot k\omega_o t} e^{j\cdot(\phi_k+\varphi_k)} + W_1(t) \quad (6)$$

$$V_{Filter2}(t) = D + \sum_{k=\pm 1}^{\pm H} |D_k H_2(jk\omega_o)| e^{j\cdot k\omega_o t} e^{j\cdot(\phi_k+\psi_k)} + W_2(t) \quad (7)$$

Where D is the offset voltage, which is approximately the same for both signals. The frequency response of the filters are $H_1(j\omega)$ and $H_2(j\omega)$, respectively:

$$H_1(j\omega) = |H_1(j\omega)| e^{\varphi(\omega)} \quad (8)$$

$$= \frac{R_3 \| R_4}{R_1 + R_2 + R_3 \| R_4} \quad (9)$$

$$H_2(j\omega) = |H_2(j\omega)| e^{\psi(\omega)} \quad (10)$$

$$= \frac{1}{(\frac{R_1}{R_4} + \frac{R_2}{R_4} + 1) + j\omega \cdot \begin{bmatrix} R_1C_1(\frac{R_2}{R_4} + 1) \\ + C_2(R_1 + R_2) \end{bmatrix} + (j\omega)^2 R_1R_2C_1C_2} \quad (11)$$

The detailed descriptions regarding filters will be discussed later.

2.2 Fundamental Amplitude Match

In order for the algorithm to work properly, both fundamental signals after two filters need to have the same amplitude, which can be interpreted as two input signals of the ADC need to have approximately the same amplitude. To achieve this, the measured resistor and capacitor with values that are close to designed values are chosen. Since any level of non-coherency is allowed, by adjusting the input frequency and compare the two ADC outputs, two outputs amplitude can be matched, with only several ADC LSBs error. Caution must be taken to avoid signal amplitude clipping when the ADC is sampling both filters output.

In designing the filters, passive components will be used on board, these devices will most likely be from the specification by possibly about 5%. This is not a problem since input frequency is allowed to adjust for fundamental amplitude matching. And the exact resistors/capacitors values are not critical, because in the algorithm, the measured values of the filters will be used to calculate filter transfer function in eq. (8)-(11) with sufficient accuracy, which minimizes the estimation error. But the mismatch between measured and designed resistors/capacitors values determines how much deviation between designed corner frequency and actual corner frequency. In addition, the algorithm itself has no restriction over input frequency, which is capable of generating a wide frequency range of high purity sinusoidal signals. An array of capacitors can be implemented to adjust filter response according to input frequency.

Another requirement for the filters is that the chosen resistors and capacitors need to have good linearity performance. This is because the algorithm cannot differentiate the nonlinearities of the filter from the nonlinearities of both the DAC and the ADC. As a result, if the filters introduce non-negligible nonlinearities, the estimation results could be erroneous.

With amplitude matched, the ADC outputs are given by:

$$V_{out1}[n] = D + \sum_{k=\pm 1}^{\pm H} |D_k H_1(jk\omega_o)| e^{j\cdot k\omega_o nT_{sADC}} e^{j\cdot(\phi_k+\varphi_k)} + \sum_{k=\pm 2}^{\pm H} |HD_k| e^{j\cdot k\omega_o nT_{sADC}} e^{j\cdot k(\phi_1+\varphi_1)+\gamma_k} + W_{ADC1}[n] \quad (12)$$

$$V_{out2}[n] = D + \sum_{k=\pm 1}^{\pm H} |D_k H_2(jk\omega_o)| e^{j\cdot k\omega_o nT_{sADC}} e^{j\cdot(\phi_k+\psi_k)} + \sum_{k=\pm 2}^{\pm H} |HD_k| e^{j\cdot k\omega_o nT_{sADC}} e^{j\cdot k(\phi_1+\psi_1)+\gamma_k} + W_{ADC2}[n] \quad (13)$$

Where higher order harmonics caused by the interaction between harmonics of the source and that of the ADC are neglected as they contribute much smaller harmonics terms compared with source and ADC harmonics. This is also analyzed and verified in [14].

2.3 Fundamental Phase Match

For the algorithm to work properly, the fundamental phase also needs to be matched for both outputs of the ADC. Since the input codes of the Main DAC for two sets of data are the same, the output after both filters are different due to different phase shift of the filter transfer function. To achieve best phase matching possible, first, after acquiring the RR attenuator output from ADC $V_{out1}[n]$, the first 5 consecutive points can be chosen, given by $x_1[1], x_1[2], x_1[3], x_1[4], x_1[5]$, it needs to be chosen from the data points that are settled, which means the initial data points that are in transient process will be discarded. Second, after acquiring the RC filter output of the ADC with the same length compared with RR attenuator output of the ADC, the first quarter portion of the data is chosen, and among these points, the best matching with first 5 points of the RR attenuator can be found by minimizing the square root mean:

$$\sqrt{\begin{matrix}(x_2[i]-x_1[1])^2 + (x_2[i+1]-x_1[2])^2 + (x_2[i+2]-x_1[3])^2 \\ + (x_2[i+3]-x_1[4])^2 + (x_2[i+4]-x_1[5])^2\end{matrix}}\Bigg|_{Min} \quad (14)$$

After the index i is found, the new RC filter output data is starting from i to the end M, which is the total data record length, with data record length $M-i+1$, and the RR attenuator output is also shorten to $M-i+1$, from $x_1[1]$ to $x_1[M+i-1]$. Here the phase difference introduced by harmonics are small enough to be negligible compared with the phase difference of the fundamental, therefore, once the ADC output data's phase is matched, it means that the fundamental initial phase is matched. Two new sets are given by:

$$V_{out1\_new}[n] = D + |D_1 H_1(j\omega_o)| e^{j\omega_o n T_{sADC}} e^{j\cdot(\phi_1+\varphi_1)} + |D_{-1} H_1(-j\omega_o)| e^{-j\omega_o n T_{sADC}} e^{j\cdot(\phi_1+\varphi_1)} + \sum_{k=\pm 2}^{\pm H} |D_k H_1(jk\omega_o)| e^{j\cdot k\omega_o n T_{sADC}} e^{j\cdot(\phi_k+\varphi_k)} + \sum_{k=\pm 2}^{\pm H} |HD_k| e^{j\cdot k\omega_o n T_{sADC}} e^{j\cdot k(\phi_1+\varphi_1)+\gamma_k} + W_{ADC1}[n] \quad (15)$$

$$V_{out2\_new}[n] = D + |D_1 H_2(j\omega_o)| e^{j\omega_o n T_{sADC}} e^{j\cdot(\phi_1+\varphi_1)} + |D_{-1} H_2(-j\omega_o)| e^{-j\omega_o n T_{sADC}} e^{j\cdot(\phi_1+\varphi_1)} + \sum_{k=\pm 2}^{\pm H} |D_k H_2(jk\omega_o)| e^{j\cdot k\omega_o n T_{sADC}} e^{j\cdot(\phi_k+\psi_k+k\cdot(\varphi_1-\psi_1))} + \sum_{k=\pm 2}^{\pm H} |HD_k| e^{j\cdot k\omega_o n T_{sADC}} e^{j\cdot k(\phi_1+\varphi_1)+\gamma_k} + W_{ADC2}[n] \quad (16)$$

Now that the initial phase is matched, meaning that the fundamental of two different filter outputs entering the ADC are approximately the same, but with different nonlinearities. Since the nonlinearities power is small compared with that of the fundamental, therefore, the differences they caused are small enough to be negligible and thus it's assumed the two filter output signals entering the ADC are approximately the same, as a result, the errors caused by ADC, which are mainly nonlinearities, are the same.

2.4 Non-coherent Fundamental Identification

The first step of the algorithm involves fundamental identification and removal, which is similar to the FIRE method [8]. The FIRE method is developed under the assumption that the harmonics power are much smaller than the power of the fundamental, although the harmonics power leakage due to non-coherent sampling will be overlap with fundamental power leakage, their spectral leakage is below the noise floor, so that the fundamental estimation will not be affected by the leakage of the harmonics. In addition, the error in estimating the power of harmonics using DFT is mainly due to the non-coherency of the fundamental [7]. However, this assumption is no longer true if the harmonics power reaches certain level, in that case, the power leakage of the harmonics will be above the noise floor, and it will introduce error to fundamental estimation, and if the fundamental estimation is inaccurate, the fundamental removal is not complete, which will in return introduce error to harmonics power estimation. Thus an iterative method introduced in [15] is used for fundamental and harmonics estimation. The detailed steps are not repeated in this paper.

After the identification, the estimated fundamental is given by:

$$\hat{V}_{Fund}[n] = \hat{A}\sin(\frac{2\pi(J_{\text{int}}+\hat{\delta})}{M}n + \hat{\phi}) + V_{os} \quad (17)$$

Where J_{int} stands for the integer part of sampled periods, $\hat{\delta}$ is the estimated fractional part of sampled periods, $\hat{A}$ is the estimated fundamental amplitude, $\hat{\phi}$ is the estimated initial phase and V_{os} is the estimated DC offset.

2.5 DAC Nonlinearity Estimation

After the fundamental in both outputs are estimated, they are subtracted from two outputs.

$$r_1[n] = V_{out1\_new}[n] - \hat{V}_{Fund}[n] \quad (18)$$

$$r_2[n] = V_{out2\_new}[n] - \hat{V}_{Fund}[n] \quad (19)$$

Since two outputs have the same ADC nonlinearities, when subtracting two residues, the ADC nonlinearities are subtracted, leaving only DAC's nonlinearities.

$$R_3[n] = r_1[n] - r_2[n] \quad (20)$$

Now in $R_3[n]$, it can be viewed as summations of a fundamental and harmonics in the form of sines and cosines. By using least square again, without the error introduced by the leakage of the fundamental, the accurate estimation of each harmonic component can be obtained similarly. Again the detailed steps are not repeatedly shown here. The estimated harmonics are given by:

$$xh_2[n] = \sum_{k=2}^{H} \begin{bmatrix} \hat{a}_k \cos(2\pi k \frac{(J_{\text{int}}+\hat{\delta})}{M} n) \\ +\hat{b}_k \sin(2\pi k \frac{(J_{\text{int}}+\hat{\delta})}{M} n) \end{bmatrix} \quad (21)$$

The estimated k^{th} harmonic component is given by:

$|\sqrt{\hat{a}_k^2+\hat{b}_k^2}|e^{j\theta_k}$, where $\theta_k = \tan^{-1}(\frac{\hat{b}_k}{\hat{a}_k})$

By subtracting (15) and (16) from (6) and (7), respectively, the ADC introduced errors are subtracted, so do the fundamental and DC component, leaving only subtractions of nonlinearities from two outputs. For $k = 2,3...H$, each k^{th} nonlinearity subtraction is obtained by $|\sqrt{\hat{a}_k^2+\hat{b}_k^2}|e^{j\theta_k}$ derived above. Ignoring the noise effect, and by re-arranging terms, the DAC nonlinearity can therefore be estimated:

$$2|\hat{D}_k| e^{j\cdot\hat{\phi}_k} = \frac{|\sqrt{\hat{a}_k^2+\hat{b}_k^2}|e^{j\theta_k}}{|\hat{H}_1(jk\omega_o)|e^{j\cdot(\hat{\varphi}_k-k\hat{\varphi}_1)} - |\hat{H}_2(jk\omega_o)|e^{j\cdot(\hat{\psi}_k-k\hat{\psi}_1)}} \quad (22)$$

Where k^{th} DAC's harmonic amplitude and phase is: $2|\hat{D}_k|, \hat{\phi}_k$.

2.6 Cal DAC Calibration

Now the Cal DAC input codes will be the estimated Main DAC nonlinearity, divided by an estimated attenuation factor $\hat{G}$.

$$C_{CDAC}(t) = round\left(\begin{pmatrix} -\hat{G}\times\sum_{k=2}^{H} 2\,|\,\hat{D}_k\,|\cos(k\omega_o t+\hat{\phi}_k) \\ +\frac{V_{RDAC}}{2} \end{pmatrix}\times 2^{N_{DAC}}\right) \quad (23)$$

Similar to Main DAC output, the Cal DAC output is given by:

$$V_{outC}(t) \approx \frac{V_{RDAC}}{2} + \left(-\hat{G}\right)\times\sum_{k=2}^{H} 2\,|\,\hat{D}_k\,|\cos(k\omega_o t+\hat{\phi}_k)$$
$$+\sum_{k=2}^{H} A_{CDACk}\cos(k\omega_o t+\phi_{CDACk}) + W_{CDAC}(t) \quad (24)$$

Where $W_{CDAC}(t)$ contains noise and quantization error of the Cal DAC.

After the attenuation, the buffered Cal DAC output is given by:

$$V_{Buffer\_C}(t) = D_C - \frac{\hat{G}}{G}\times\sum_{k=\pm 2}^{\pm H}|\,\hat{D}_k\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\hat{\phi}_k} + E_{CDAC}(t)/G \quad (25)$$

$$E_{CDAC}(t) = \sum_{k=2}^{H} A_{CDACk}\cos(k\omega_o t+\phi_{CDACk}) + W_{CDAC}(t) \quad (26)$$

As can be seen from eq.(25), the error introduced by the Cal DAC is attenuated by the factor of G, the error introduced by Cal DAC itself will be small enough, so that the combined DAC output signal will not be affected by the Cal DAC errors.

One thing to be mentioned is that the attenuation needs to be controlled to some level so that the input codes range will near the full range of the Cal DAC input. However, if the attenuation factor is too large, the Cal DAC input will be clipped, which will lead to wrong output and not only the nonlinearities of the Main DAC will not be cancelled, but also will introduce extra distortions to the combined signal.

After the attenuation, the combined DACs output is given by:

$$V_C(t) = D_0 - D_C + |\,D_1\,|\,(e^{j\cdot k\omega_o t}+e^{-j\cdot k\omega_o t})e^{j\cdot\phi_k}$$
$$+\sum_{k=\pm 2}^{\pm H}\left(|\,D_k\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\phi_k} - (1+GE_F)\times\left(-\frac{\hat{G}}{G}\right)\times|\,\hat{D}_k\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\hat{\phi}_k}\right)$$
$$+W_{MDAC}(t) - E_{CDAC}(t)/G \quad (27)$$

Once the input codes are fed into Main DAC and the devices are turned on accordingly, the whole iteration of generating Cal DAC codes can be automatically performed to produce ultra-pure sine wave. Therefore, it is capable of self-calibration.

2.7 Ultra-High Pure Signal Capturing

The combined signal now should have most of the nonlinearities cancelled. A high resolution ADC can be used to capture this high purity combined signal. Band-pass filter can also be used to filter output other frequency component except for fundamental signal. If the purity of the combined signal is beyond the purity of the ADC that is used to capture it, alternatively, the high purity of the combined signal can be demonstrated by accurately evaluating the performance of high performance ADC under test.

If the signal still has residual nonlinearities left, as mentioned before, more iterations can be used to improve the signal purity.

2.8 Iterations & Convergence

In this section, mathematical analysis will be shown to demonstrate that the iteration process is guaranteed to converge and the source nonlinearity will be eventually calibrated that only limited by noise.

Let $HD_{k,i}$ stands for k[th] input harmonic distortion in i[th] iteration ($i = 1,2,\cdots$). At 1[st] iteration, the true value of k[th] input harmonic distortion is: $HD_{k,1} = |\,D_k\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\phi_k}$

And the estimated k[th] input harmonic distortion is given by:

$$HD_{k,1} = |\,\hat{D}_{k,1}\,|\,e^{j\cdot\hat{\phi}_{k,1}} \quad (28)$$

$$= \frac{|\sqrt{\hat{a}_{k,1}^2+\hat{b}_{k,1}^2}\,|\,e^{j\hat{\theta}_{k,1}}}{2\left(|\,\hat{H}_1(jk\omega_o)\,|\,e^{j\cdot(\hat{\phi}_k-k\hat{\phi}_1)} - |\,\hat{H}_2(jk\omega_o)\,|\,e^{j\cdot(\hat{\psi}_k-k\hat{\psi}_1)}\right)} \quad (29)$$

At 2[nd] iteration, the true value of k[th] input harmonic distortion is given by:

$$HD_{k,2} = HD_{k,1} - \frac{\hat{G}}{G}\times HD_{k,1} + \frac{|\,D_{CDACk}\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\phi_{CDACk}}}{G} \quad (30)$$

Therefore, at (i+1)[th] iteration, the k[th] harmonic distortion is:

$$HD_{k,i+1} = HD_{k,i} - \frac{\hat{G}}{G}\times HD_{k,i} + \frac{|\,D_{CDACk}\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\phi_{CDACk}}}{G} \quad (31)$$

Assume $HD_{k,i} = HD_{k,i} + \Delta HD_{k,i}$ (32)

where $\Delta HD_{k,i}$ contain the i[th] iteration's estimation. Then eq.(31) can be rewritten as:

$$HD_{k,i+1} = (1-\frac{\hat{G}}{G})HD_{k,i} + \frac{\hat{G}\cdot\Delta HD_{k,i} + |\,D_{CDACk}\,|\,e^{j\cdot k\omega_o t}e^{j\cdot\phi_{CDACk}}}{G} \quad (33)$$

$HD_{k,i}$ can also be given by:

$$HD_{k,i} = \frac{|\sqrt{a_{k,i}^2+b_{k,i}^2}\,|\,e^{j\theta_{k,i}}}{2\left(|\,H_1(jk\omega_o)\,|\,e^{j\cdot(\varphi_k-k\varphi_1)} - |\,H_2(jk\omega_o)\,|\,e^{j\cdot(\psi_k-k\psi_1)}\right)}$$
$$+W_{HD\_ADC+N} \quad (34)$$

Where W_{HD_ADC+N} contains the ADC harmonics and noise subtraction between two ADC outputs, and error from true and estimated filters values.

On the numerator, $|\sqrt{a_{k,i}^2+b_{k,i}^2}\,|\,e^{j\theta_{k,i}}$ is linearly proportional to $HD_{k,i}$, let: $|\sqrt{a_{k,i}^2+b_{k,i}^2}\,|\,e^{j\theta_{k,i}} = \beta\cdot HD_{k,i}$, and

$\frac{1}{\alpha} = 2\left(|\,H_1(jk\omega_o)\,|\,e^{j\cdot(\psi_k-k\psi_1)} - |\,H_2(jk\omega_o)\,|\,e^{j\cdot(\varphi_k-k\varphi_1)}\right)$,

which is independent of iterations.

Similarly, let $\alpha = \hat{\alpha} + \Delta\alpha$, $\beta = \hat{\beta} + \Delta\beta$. $\Delta\alpha$ contains the estimation error from slightly inequality of two outputs ADC nonlinearity; $\Delta\beta$ contains the estimation error from FIRE and Least Square computational errors.
Then eq.(34) can be written as:

$$HD_{k,i} = \alpha \cdot \beta \cdot HD_{k,i} + W_{HD\_ADC+N} \quad (35)$$

$$\approx HD_{k,i} + (\Delta\alpha + \Delta\beta) \cdot HD_{k,i} + W_{HD\_ADC+N} \quad (36)$$

Plugging eq.(36) into eq.(33), we have:

$$|HD_{k,i+1}| = \left|\frac{\Delta G + \hat{G}\cdot(\Delta\alpha + \Delta\beta)}{G}\right| \cdot |HD_{k,i}| + \left|\frac{\hat{G}\cdot W_{HD\_ADC+N} + |D_{CDACk}| e^{j\cdot k\omega_o t} e^{j\cdot\phi_{CDACk}}}{G}\right| \quad (37)$$

Where $0 < \left|\frac{\Delta G + \hat{G}\cdot(\Delta\alpha + \Delta\beta)}{G}\right| \ll$, and

$\varepsilon = \left|\frac{\hat{G}\cdot W_{HD\_ADC+N} + |D_{CDACk}| e^{j\cdot k\omega_o t} e^{j\cdot\phi_{CDACk}}}{G}\right|$ is the small error term due to various error sources mentioned earlier.
Therefore, we have: $\lim_{i\to\infty} |HD_{k,i}| = \varepsilon$ (38)

It demonstrates that as iteration process continues, eventually the source nonlinearity will be calibrated and converges.

3. Simulation Results

The proposed method is first validated by simulations done in MATLAB. A 16 bit nonlinear ADC with THD of -85dB and two 16 bit nonlinear DACs (THD of -85dB) are modeled in MATLAB. The input codes are also generated in MATLAB, which is the ideal sinewave with amplitude that near the full range of ADC and DAC. The number of period J in the input codes is integer 331. Later the resistors and capacitors are modeled with 5% values mismatch, which serve as RR, RC filter component in actual circuit. The output of the Main DAC is then transformed via FFT to frequency domain and multiply the transfer function of both filters. The time domain output of both filters can be acquired by taking the IFFT of the modified output data. These steps will model the output time domain signal after the filters, which will be the input of the ADC. Because the filter component has mismatch, after obtaining two outputs from the ADC, the calibrations steps described in section II.B are used to match the amplitude of both ADC outputs. The frequency of the input is now changed, meaning that J will no longer be an integer, the signal will be non-coherently sampled by the ADC. This will not introduce additional problem since the algorithm can tolerate any level of non-coherency. After using the algorithm, two DACs outputs are combined to obtain the combined ultra pure signal, and two iterations are performed in the simulation.
Figure 2 shows the spectrum of orignal Main DAC output(Red), and the generated ultra-pure signal output by proposed method (Blue and Green), 2 iteration results are

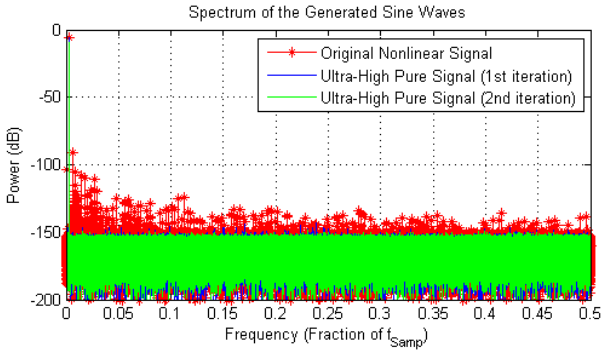

Figure 2: Spectrum of the generated sine waves

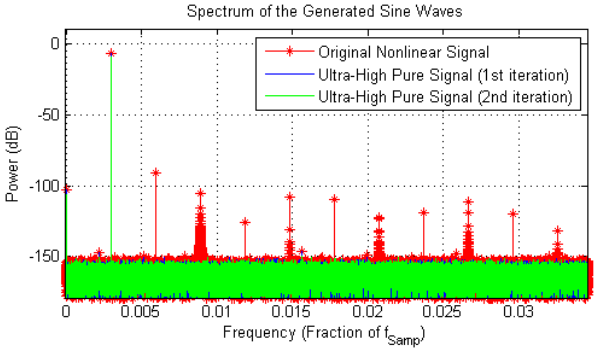

Figure 3: Zoomed spectrum of the generated sine waves showing fundamental and first 10 harmonics in Figure 2

shown, respectively. Figure 3 shows the zoomed spectrum for fundamental and first 10 harmonics. In simulation, the true spectrum of the signal is obtained by taking the FFT of the signal, assuming the ADC that caputure these signals has infinite resolution. In actual measurment, which will be discussed in details in section IV, this generated ultra-pure signal is used to test a commerial high performance ADC. It can be seen from Figure 2 that after 1st iteration, most of the harmonics are cancelled, but still there're some at higher frequencies that are not accurately estimated and complelely removed (Blue). After 1st iteration the residue harmonics that were failed to be captured are removed during 2nd iteration (Red), resulting the signal purity (THD) around -140dB.

4. Measurement Results

A Print Circuit Board (PCB) is designed to validate the proposed method, which is shown in Figure 4. The motherboard is shown (Figure 4 above), with an Opel Kelly FPGA connected to PC via an USB 2.0 connector. This FPGA is used to generate common mode signals and other control signals. The ultra-pure sine wave board is the board that is custom designed for this project housing two DACs (DAC8831), filter block and a 18-bit ADC (ADS9110). Main DAC (DAC8831) is used to a 2kHz and 4.169kHz impure sinusoidal signal with 1.25 or 2.5Vpp. High precision/low distortion capacitors and resistors are used to design the RR and RC filter. For RR attenuator, the resistor values are: R1=R2 =1.1k, R3=2.2k; for RC filter, the capacitor values are: C1=C2=47nF.

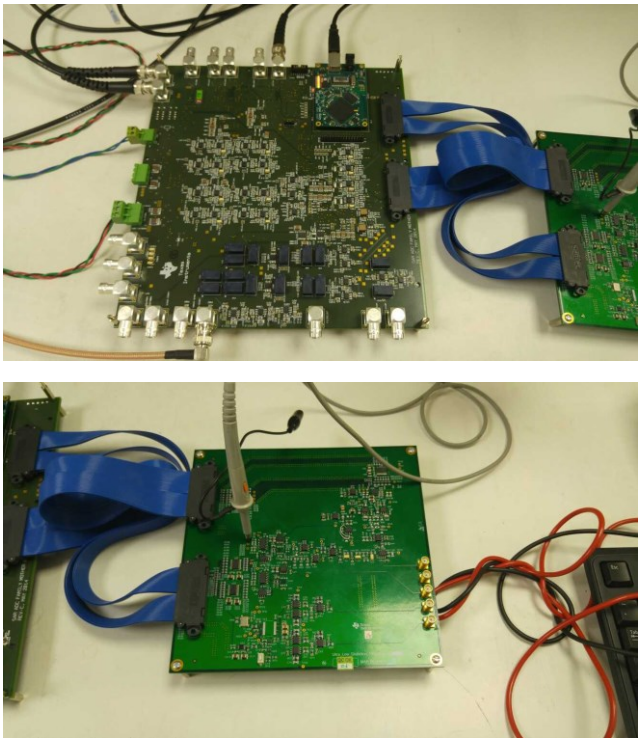

Figure 4: Designed printed circuit board: motherboard with FPGA (above) and custom ultra-pure sine wave board with DACs/ADC (below)

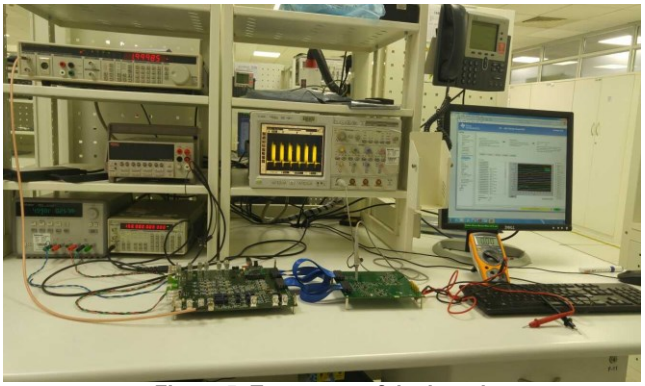

Figure 5: Test setup of the board

For DACs, the Main DAC serves as the signal generator, and the Cal DAC serves as the calibration device, there's no need to discuss mismatch between these two DACs because they serve different purposes. They could be in different structure or different resolution. The selection of the DACs depends on the frequency of the generated ultra-pure sine wave, they should be capable of generating sine wave of such frequency. There's trade-off between speed and accuracy of the DAC, for best performance of the DAC, the DAC's maximum output frequency is more than 10 times of the generated sine wave, so that the sine wave can be viewed as pseudo static. For the ADC, depending on how many orders of harmonics needed to be sampled, it should also be capable of sampling fundamental and harmonics of the input sine wave. Similarly, there's trade-off between speed and accuracy of the ADC. The buffers need to have good linearity performance. Especially the one before the ADC, which should contribute negligible nonlinearity to the system compared with source nonlinearity and ADC nonlinearity. The op amps that serve as buffers at the output of DAC and input of the ADC are OPA211.

Figure5 shows the test setup in validating the proposed method. The steps for running the test is described as follows:

1. The first step involves filter characterization, sine waves of and various harmonics frequencies are generated and pass through the filters. Accurate filters transfer function can be obtained.
2. Using approach described in section II.B, fundamental amplitude can be matched to accurate level: Labview is used to generate 2^{16} unique points for a sine wave, which are feed to Main DAC using SDI with the help of FPGA and this output is first passed through RR attenuator and then RC filter. Two outputs are captured using the ADC and frequency is adjusted slightly so that the 2 fundaments have the same amplitude. Once this frequency is determined the test can begin.
3. Sine wave with previous adjsuted frequency were generated by Main DAC, Cal DAC is fed with all zeros once DACs are settled. Two DAC outputs are combined and then passing through RR RC filters, respectively. ADC is used to capture these two outputs, respectively.
4. Proposed algorithm is used to obtain estimation of Main DAC nonlinearity, and generate Cal DAC calibration code accordingly.
5. Same input codes are given to Main DAC while Cal DAC's input is estimated Main DAC nonlinearity. The combined output is again passed through RR RC filters and ADC captures two outputs, which sends to proposed algorithm. This iterative process is repeated until the purity of the generated sine wave is sufficiently high.

Since generated sine wave possess high purity that no equipment in lab can accurately characterize it, to evaluate the generated sine wave and claim its high purity, the ADC on board (ADS9110) is used as a measurement device, which we compared the ADC output spectrum using generated sine wave as input source, with reference spectrum that uses state-of-the-art test setup, including high purity source, coherent sampling, etc. The ADC on board has low distortion, which has optimized THD of -120dB level at 2kHz input frequency. If this ADC can be tested accurately by generated sine wave, the input source purity is 15~20dB beyond distortions of the ADC, and hence it can be demonstrated to have ultra-high purity.

Figure 6 shows the spectrum results of ADS9110, using generated sine wave and state-of-the-art source, which serves as the reference. The input frequency is around 2kHz for generated sine wave with 1.25Vpp. For reference, the input frequency has to be precisely controlled (2.00081kHz) to achieve coherent sampling. It can be seen that both blue and red spectrum match well on fundamental, harmonics bins and noise level. Table 1 further validates the accuracy of proposed method as the spectral performance of the ADC under test is close to the reference. Figure 7 shows another

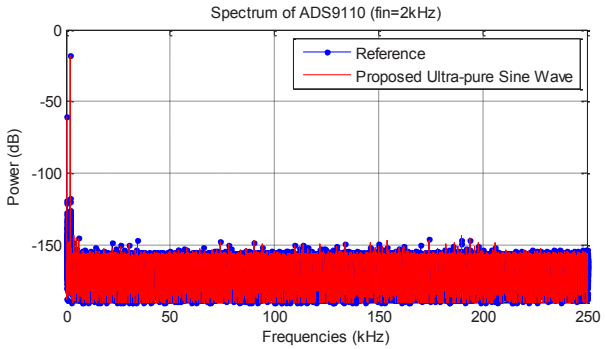

Figure 6: ADS9110 (fin=2kHz) spectrum using: (blue) reference, (red) generated sine wave as input

Table 1. Spectral Specifications of ADS9110 (fin=2kHz)

Input Signal	THD(dB)	SFDR(dB)	SNR(dB)
Reference	-120.42	124.85	97.13
Proposed	-120.05	124.31	96.74

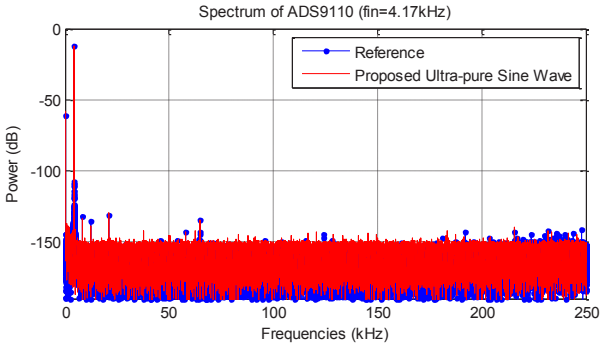

Figure 7: ADS9110 (fin=4.17kHz) spectrum using: (blue) reference, (red) generated sine wave as input

Table 2. Spectral Specifications of ADS9110 (fin=4.17kHz)

Input Signal	THD(dB)	SFDR(dB)	SNR(dB)
Reference	-115.61	118.05	97.35
Proposed	-114.98	117.64	96.88

set of results, and Table 2 shows the spectral performance of ADC under test, whose input frequency is around 4.17kHz with 2.5Vpp, while reference frequency is precisely controlled to be 4.16946kHz. Similarly, spectrum and the spectral performance of ADC under test matches well after using generated ultra-pure sine wave with the reference. These two sets of measurement results have demonstrated that the generated sine wave possess ultra-high purity that is beyond -120dB and is capable of accurately obtaining spectral performance of high performance ADCs.

5. Conclusions

A new method that is capable of generating ultra-pure sine wave using two DACs and an ADC with distortions that are thousands time worse than the generated signal was proposed. The proposed method performs in-situ calibration by innovatively estimating and removing distortions present in the generated sine wave through iterations. Simulation results demonstrated that the generated signal purity approaches -140dB. And measurement results showed that the generated sine wave is capable of testing an ADC with -120dB THD accurately, which again demonstrated its high purity. The proposed method can also tolerate any level of non-coherency, making it robust against non-coherent sampling. The main advantage of this method is that it performs in-situ calibration and generates an ultra-pure sine wave using low-cost DACs and ADCs, which can be utilized in various high precision circuitry and systems with much lower test setup cost.

6. Acknowledgements

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