Prof. Willy Sansen w AGH z cyklem wykładów z elektroniki

Zapraszamy studentów, doktorantów i pracowników Akademii Górniczo-Hutniczej na dwudniowy cykl wykładów, które wygłosi prof. Willy Sansen. Wykłady odbędą się w dniach 12-13 października 2015 r. na Wydziale Elektrotechniki, Informatyki i Inżynierii Biomedycznej (bud. B-1, s. 121).

Circuits with resistor and capacitor cancellation: design techniques to enhance high-frequency performance without increased power consumption

- **Program wykładów (.pdf, 234 KB)**

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- **9:00 - 10:30 Minimum-power amplifying stages**
  Single-transistor stages determine the performance for high-frequency blocks such as LNA's and VCO's. Moreover they determine the gain, which can be realized in nanometer CMOS transistor stages. The gain, input and output impedance is analyzed of the three single-transistor stages i.e. the amplifier, the source follower and the cascode. In addition the current consumption is minimized of the amplifying stage using EKV/BSIM6 models.
- **11.00-12.30 Differential amplifying blocks with positive feedback**
  Practical designs are built up by means of differential pairs, current sources and two-transistor cascodes. They are analyzed in details followed by fullydifferential voltage and current amplifiers. Positive feedback is added as well to enhance both the Gain and the Gain-Bandwidth. Design procedures are discussed in all regions of operations (from weak to strong inversion and velocity saturation).
- **13.30-15.00 High-frequency and RF design techniques**
  Real high-frequency performance can be reached up to f /3 even if all parasitic components are included. In addition feedforward and pole-zero compensation T schemes can be adopted to extend the frequency range. Many examples are given and discussed.
- **15.30-17.00 Examples of low-noise design**
  Low-noise design techniques are applied to amplifier configurations, filters and LNA's. Indeed wireless receivers all start with a LNA (Low-noise amplifier) to provide limited gain but with low noise and distortion. The most recent ones are all wide-band, and use both noise and distortion cancellation, which yields higher FOM's than hitherto possible.

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- **9.00-10.30 Compensation techniques in operational amplifiers**
  Two-stage operational amplifiers in unity-gain configuration, suffer from peaking unless a compensation capacitance is added, or the current is increased in the second stage. These stability

conditions are examined followed by three techniques to get rid of the positive zero. These design plans are extended to threestage amplifiers with nested Miller compensation.

- **11.00-12.30 Most-important opamp configurations**
  In practice only a few amplifier configurations are used. Examples are the symmetrical amplifier, the folded-cascode and the Miller OTA amplifier. In this presentation, all of them are optimized with respect to power consumption, high-speed capability and noise. The compromises are discussed in detail and a comparison is provided. In addition, some specific design techniques such as negative resistors, are reviewed to enhance performance.
- **13.30-15.00 Design of multistage operational amplifiers**
  Two-stage amplifiers may not provide sufficient gain and or frequency performance in nanometer CMOS technologies. This is why three-stage amplifiers have become necessary. This is also true for most power amplifiers in which two preceding stages are required for high gain. The stability is analyzed of such amplifiers. It is shown that three-stage amplifiers can provide tracking pole-zero compensation, which results in lower power consumption than a two-stage amplifier with similar performance.
- **15.30-17.00 Opamps, Gm-block or Inverters for filters**
  Operational amplifiers have been the backbone of most amplifiers and filters in communication applications and ADCs. They are in competition with Gm blocks for higher frequencies despite their higher linearity. Both of them are now gradually being replaced by CMOS inverters. This presentation focuses on the merits and advantages of all three of them.

Kurs odbywający się w ramach najbliższego spotkania IEEE Solid-State Circuits Society Chapter Poland został zorganizowany pod patronatem Rektora AGH prof. Tadeusza Słomki.