IEEE Solid-State Circuits Society Poland Chapter
together with Department of Measurement and Electronics
invites for

Lectures given by IEEE SSCS Distinguished Lecturers

Friday, October 21st, 2016, 13:30 - 18:00
Coffee Break at 15:00
AGH building A-0, 1st floor, Auditorium Hall

ATTENDANCE FREE OF CHARGE

ALL STUDENTS ARE WELCOME

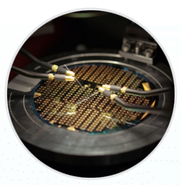
Embedded flash memory: technology, circuits to systems and MCU/SOC applications

by Hideto Hidaka

Since its inception in early 1990's, embedded flash memory (eFlash) for MCU applications has realized a revolutionary advancements by programmable instruction functions, which has proliferated in all the segments in MCU market for embedded system applications and has reached 28nm development today. This eFlash innovation has its roots in reducing the overall cost of products and embedded system development by programmable instruction functions to support consistent market growth.

Break-through technology and applications in automotive, security, and low-power applications are reviewed with insights into future prospects of application-driven non-volatile memory technology in the era of advanced automotive systems and of IoE (Internet of Everything). Trials on technology convergence scheme and future prospects of embedded non-volatile memory in the new memory hierarchy are also described.

1. MCU with eFlash technology; history and prospects over 20 years
2. Family of eFlash technology and use cases, eFlash innovation study
3. eFlash technology, architecture, circuits and sub-system design evolution
4. Meaning of non-volatility and programmability and its impact on the VLSI evolutions
5. Trends and future prospects in eFlash and eNVM required by auto-motive, cellular phone, and emerging IoE applications



Basics of Asynchronous Circuits Design

by Makoto Ikeda

This lecture will overlook basics and variety of asynchronous controlling, from the view point of advantages for low-voltage & variation rich conditions. This lecture takes two extreme example of complete completion detection type asynchronous designs as examples and demonstrate details of operation and performance. In addition, this talk will cover recent trial on design flow of random logic by the self-synchronous circuits.

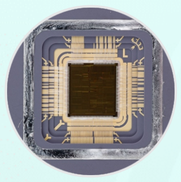
How future mobility meets IT: Embedded Cyber-Physical System

by Hideto Hidaka

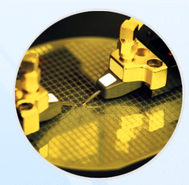
In the modern automotive technology where Control (on mobility/energy in physical-world) meets IT (by information in cyber-world), we explore every capability of efficiency /performance /cost based on existing technology, with newer system challenges. Essential new sub-system technologies triggered by functionality requirements over physical through cyber systems include; security, functional safety, sensing, and connectivity etc.

On top of these sub-system technologies shared with motor-control, Industry 4.0 by M2M, and trillion sensory systems by IoT, a new challenge for 2030 should be the extensive system-wide knowledge and design through the physical and cyber systems (CPS) in coordinated ways in order to better use variety of existing semiconductor technology. On the other hand the system design should consider different physical/human system behaviors, for instance, in auto (instant mobility, idle, shut-down) and motor control in industry (constant mobility, 24/7/365 operations) applications.

In this talk the speaker re-evaluates Si design/technology capabilities and limitations in each of the key sub-system technology for personalized mobility and IoT into an agenda plan for 2030. Also issues in multi-system design, triggering innovation, R&D funding, and education are addressed in view of the roles taken by government/academia/industry.



Basics of CMOS Image Sensors



by Makoto Ikeda

This lecture will cover the basics of CMOS image sensor processes, noise characteristics of CMOS Image sensors, including thermal noise, flicker noise, reset noise and Vth variations of readout source follower, and signal chain from pixel to column parallel ADCs to achieve low noise readout as low as 1e-. This lecture will also cover some of dynamic range extension techniques, including multiple exposure techniques, logarithmic compression techniques and frequency conversion techniques, and low power techniques.

Biographies of the invited speakers

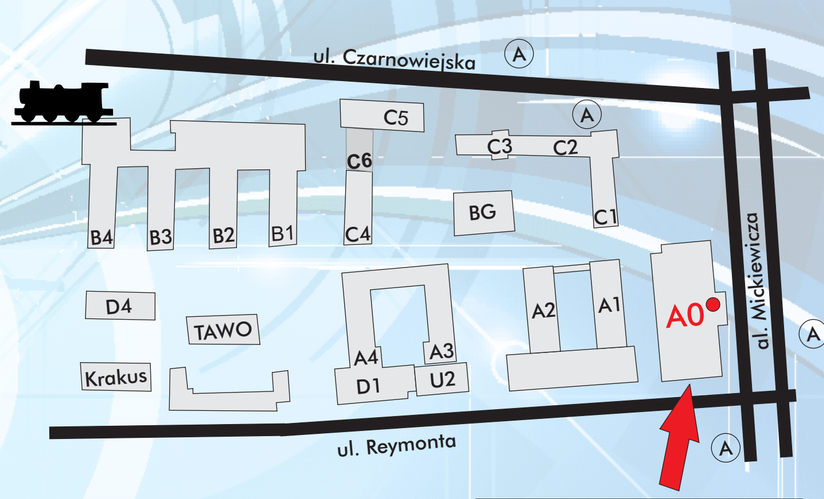
Hideto Hidaka earned the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan. In Mitsubishi Electric, Renesas Technology, and Renesas Electronics he has been engaged in the research and development of high-density, application-specific, and embedded aspects of DRAM technology and circuits, embedded-flash memory for MCU, embedded non-volatile memory technology, and related technology platforms and analog IPs for MCU and SOC products.

Since 2005 he and his team have created the world's first split-gate embedded SONOS flash memory for MCU products at 90 nm technology node, which changed the MCU technology trend for automotive applications in performance, power, and reliability advantages. He led this development into market dominance to make a de-facto standard in MCU applications, which was followed by successful 40 nm and 28 nm SONOS-eFlash development. He has consistently led the MCU technology and business strategies enabling the world's No.1 MCU market share position by Renesas Electronics now, where he was responsible for R&D in all the embedded non - volatile memories and technology platforms for MCU products. He is now the Senior Vice-President and Chief Technology Officer at Renesas Electronics Corp. responsible for all the corporate R&D activities.

He has authored and co-authored more than 60 journal papers and conference papers, as well as 293 US patents and 193 Japanese patents issued. He was a visiting scientist at the Media Laboratory, MIT, in 1987–88, and he has been a lecturer for a graduate course at the Tokyo Institute of Technology, Tokyo, in 2013–2015 Dr. Hidaka has served on program committees of technical conferences: ISSCC by the Memory Subcommittee Chair, Program Committee (ITPC) Vice-chair and Chair (2012), as well as A-SSCC, ICICDT, VLSI-TSA, IEICE-ICD, and ICDV. He is a member of the IEEE SSCS Adcom, an Associate Editor of JSSC, a Steering Committee member of Trans. VLSI Systems, an advisory board member for the IEEE SSCS Magazine, and Chair of IEEE-SSCS Kansai Chapter. He is an SSCS Distinguished Lecturer in 2015–2016

Makoto Ikeda received the BE, ME, and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1991, 1993 and 1996, respectively. He joined the University of Tokyo as a research associate, in 1996, and now professor at the department of electrical engineering and information systems. At the same time he has been involving the activities of VDEC(VLSI Design and Education Center, the University of Tokyo), to promote VLSI design educations and researches in Japanese academia. He worked for asynchronous circuits design, smart image sensor for 3-D range finding, and time-domain circuits for associate memories. He has published more than 230 technical publications, including 10 invited papers, and 7 books/chapters. He has been serving various positions of various international conferences, including ISSCC IMMD sub-committee chair (ISSCC 2015 -), A-SSCC 2015 TPC Chair, VLSI Circuits Symposium PC Chair (will be for 2016/2017). He is a member of IEEE, IEICE Japan, IPSJ and ACM.

Meeting venue
AGH University of Science and Technology
Av. Mickiewicza 30, Kraków, Poland
Building A-0, 1st floor, Auditorium Hall



Solid-State Circuits Society
SSCS.IEEE.org

Microelectronics in Industry and Medicine
www.mtm.agh.edu.pl

Dept. of Measurement and Electronics
www.kmet.agh.edu.pl