Invited Lectures by Prof. Willy Sansen

organized under auspices of His Magnificence Rector AGH Prof. dr hab. inż. Tadeusz Słomka
and the IEEE Solid-State Circuits Society Poland Chapter technical meeting

Circuits with resistor and capacitor cancellation: design techniques to enhance high-frequency performance without increased power consumption

Monday, Oct. 12th, 2015, building B1, room 121

9:00 - 10:30 Minimum-power amplifying stages
Single-transistor stages determine the performance for high-frequency blocks such as LNA's and VCO's. Moreover they determine the gain, which can be realized in nanometer CMOS transistor stages. The gain, input and output impedance is analyzed of the three single-transistor stages i.e. the amplifier, the source follower and the cascode. In addition the current consumption is minimized of the amplifying stage using EKV/BSIM6 models.

11.00-12.30 Differential amplifying blocks with positive feedback
Practical designs are built up by means of differential pairs, current sources and two-transistor cascodes. They are analyzed in details followed by fully-differential voltage and current amplifiers. Positive feedback is added as well to enhance both the Gain and the Gain-Bandwidth. Design procedures are discussed in all regions of operations (from weak to strong inversion and velocity saturation).

13.30-15.00 High-frequency and RF design techniques
Real high-frequency performance can be reached up to $f_T/3$ even if all parasitic components are included. In addition feedforward and pole-zero compensation schemes can be adopted to extend the frequency range. Many examples are given and discussed.

15.30-17.00 Examples of low-noise design
Low-noise design techniques are applied to amplifier configurations, filters and LNA's. Indeed wireless receivers all start with a LNA (Low-noise amplifier) to provide limited gain but with low noise and distortion. The most recent ones are all wide-band, and use both noise and distortion cancellation, which yields higher FOM's than hitherto possible.

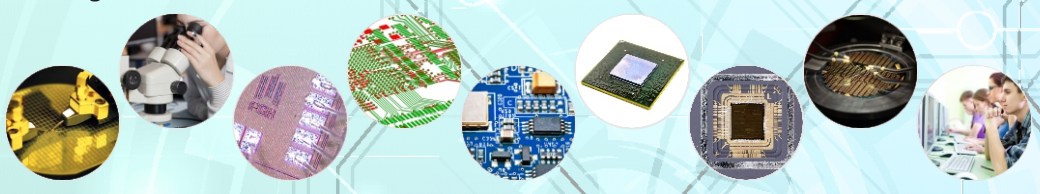
Tuesday, Oct. 13th, 2015, building B1, room 121

9.00-10.30 Compensation techniques in operational amplifiers
Two-stage operational amplifiers in unity-gain configuration, suffer from peaking unless a compensation capacitance is added, or the current is increased in the second stage. These stability conditions are examined followed by three techniques to get rid of the positive zero. These design plans are extended to three-stage amplifiers with nested Miller compensation.

11.00-12.30 Most-important opamp configurations
In practice only a few amplifier configurations are used. Examples are the symmetrical amplifier, the folded-cascode and the Miller OTA amplifier. In this presentation, all of them are optimized with respect to power consumption, high-speed capability and noise. The compromises are discussed in detail and a comparison is provided. In addition, some specific design techniques such as negative resistors, are reviewed to enhance performance.

13.30-15.00 Design of multistage operational amplifiers
Two-stage amplifiers may not provide sufficient gain and or frequency performance in nanometer CMOS technologies. This is why three-stage amplifiers have become necessary. This is also true for most power amplifiers in which two preceding stages are required for high gain. The stability is analyzed of such amplifiers. It is shown that three-stage amplifiers can provide tracking pole-zero compensation, which results in lower power consumption than a two-stage amplifier with similar performance.

15.30-17.00 Opamps, Gm-block or Inverters for filters
Operational amplifiers have been the backbone of most amplifiers and filters in communication applications and ADCs. They are in competition with Gm blocks for higher frequencies despite their higher linearity. Both of them are now gradually being replaced by CMOS inverters. This presentation focuses on the merits and advantages of all three of them.



ALL STUDENTS ARE WELCOME

Biography of the invited speaker

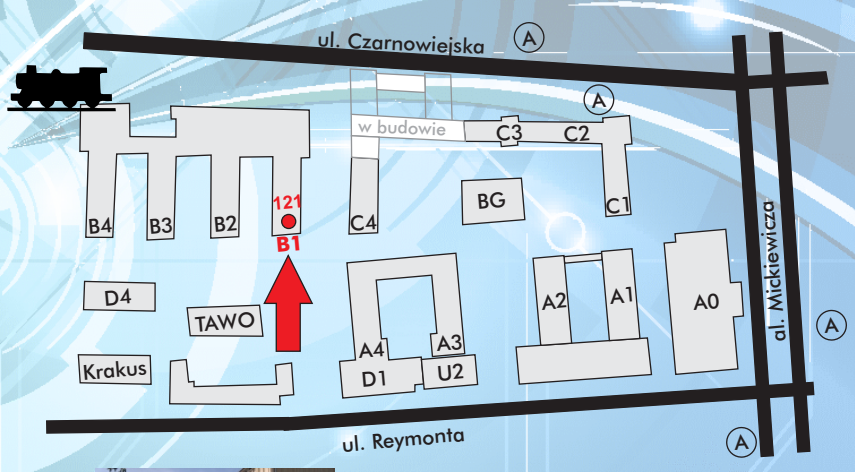
Willy Sansen has received the MSc degree in Electrical Engineering from the Katholieke Universiteit Leuven in 1967 and the PhD degree in Electronics from the University of California, Berkeley in 1972.

In 1972 he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT laboratory of the K.U.Leuven, where he has been a full professor since 1980. During the period 1984-1990 he was the head of the Electrical Engineering Department. From 1984 to 2008 he was head of the ESAT-MICAS laboratory on analog design, which counts about sixty members and which is mainly active in research projects with industry and in teaching worldwide.

In 1978 he was a visiting professor at Stanford University, in 1981 at the EPFL Lausanne, in 1985 at the University of Pennsylvania, Philadelphia, in 1994 at the T.H. Ulm and in 2004 at Infineon, Villach. Prof. Sansen is a member of several editorial and program committees of journals and conferences. He is cofounder and organizer of the workshops on Advances in Analog Circuit Design in Europe. He is a member of the executive and program committees of the IEEE ISSCC conference. He was program chair of the ISSCC-2002 conference and was President of the Solid-State Circuits Society in 2008/2009. He is a life-fellow of the IEEE.

He has been involved in design automation and in numerous analogue integrated circuit designs for telecommunications, consumer electronics, medical applications and sensors. He has been supervisor of over sixty-five PhD theses in these fields. He has authored and coauthored more than 620 papers in international journals and conference proceedings and fifteen books, among which "Analog design essentials" (Springer 2008).

Meeting venue
AGH University of Science and Technology
Av. Mickiewicza 30, Kraków, Poland
Building B1, 121 lecture hall, 1st floor



B1 Building

Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering